SY21299

8A Current Limit Step-Up Regulator

General Description

The SY21299 high efficiency step-up regulator operates using current mode control over an input voltage range from 3V to 5.5V. It integrates an N-channel MOSFET with low 65mΩ $R_{DS(ON)}$ to minimize conduction loss. A built-in internal soft-start circuitry minimizes inrush current at startup.

The device offers cycle-by-cycle overcurrent and thermal shutdown protections.

The SY21299 is available in a compact DFN3×3-10 package.

Features

- 3V to 5.5V Input Range
- 30V Maximum Output Voltage
- 1 µA Shutdown Current (Typ.)
- 380 µA Quiescent Current (Typ.)
- Programmable Peak Current Limit
- Programmable Constant Off-Time
- Low $R_{DS(ON)}$ for Internal 9A N-Channel MOSFET: 65mΩ
- Internal Soft-Start
- RoHS-Compliant and Halogen-Free
- Compact DFN3mm×3mm-10 Package

Applications

- Industrial Control Systems
- Battery Powered Devices
- LED Drivers

Typical Application

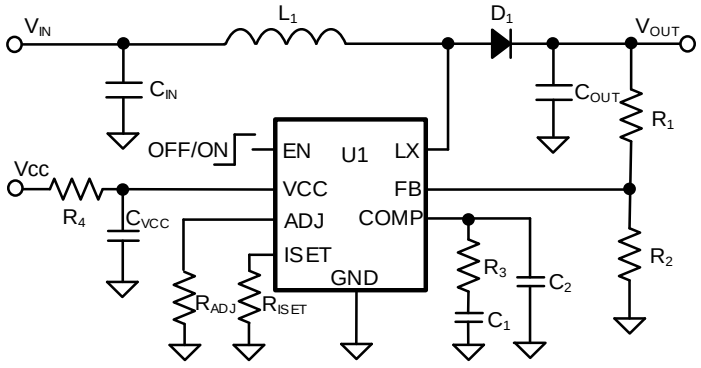

Figure 1. Typical Application Circuit

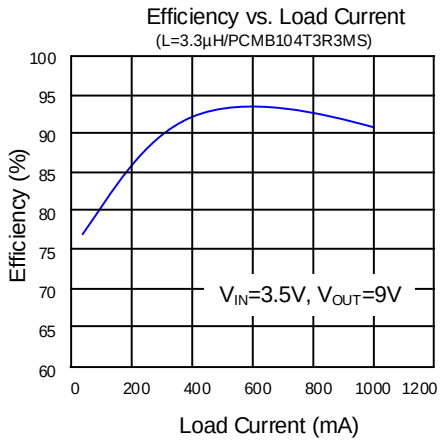

Figure 2. Efficiency vs. Output Current

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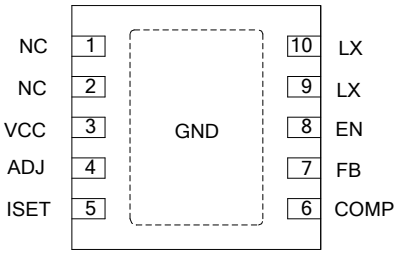
Ordering Information

Ordering Part Number	Package type	Top Mark
SY21299DBC	DFN3×3-10 RoHS-Compliant and Halogen-Free	**GV*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1, 2	NC	No connection
3	VCC	Power supply pin
4	ADJ	Connect a resistor to ground to program the t_{off} time.
5	ISET	Connect a resistor to ground to program the current limit threshold of the internal MOSFET.
6	COMP	Compensation pin. Connect an RC network between this pin and ground to program the best transient response.
7	FB	Output Feedback Pin. The reference voltage is 1.25V. If the voltage on the FB pin is higher than the reference voltage by 5%, the OVP is triggered.
8	EN	Enable control pin. Connecting this pin to VCC with a 1kΩ resistor recommended for always on applications.
9,10	LX	Switching node. Connect this pin to the switching node of the inductor.
Exposed pad	GND	Ground pin. Connect to system GND.

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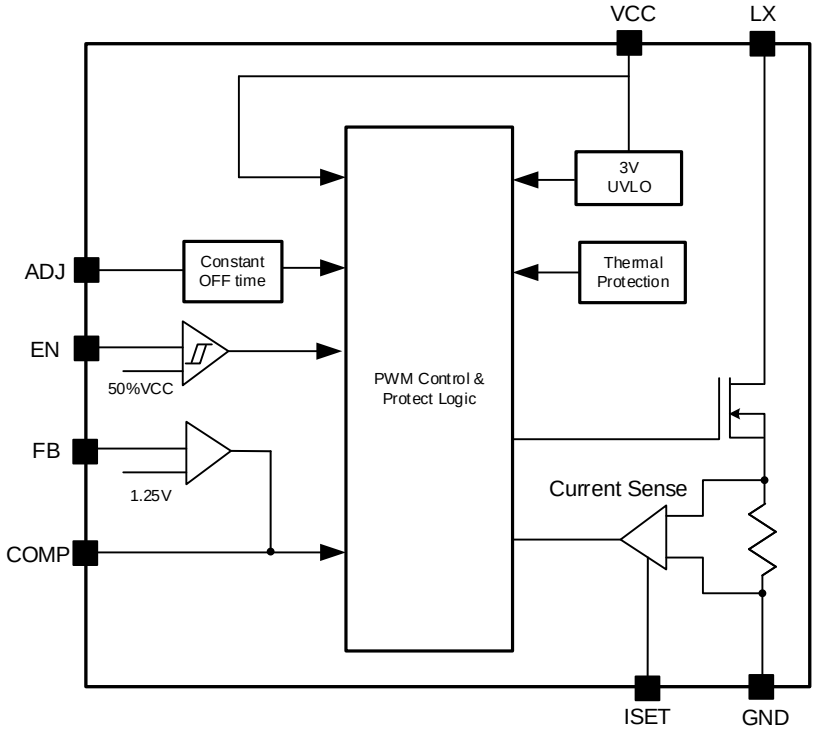
Block Diagram



Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
LX	-0.3	36	V
All Other Pins	-0.3	5.5	
LX, 50ns Duration	39	GND-4	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	125	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	38	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	8	
P_D Power Dissipation T_A=25°C	2.6	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
LX	0	30	V
EN, VCC	3	5.5	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

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Electrical Characteristics

(V_{CC} = 5.0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{CC} Input Voltage Range	V_{CC}		3		5.5	V
V_{CC} Rising UVLO Threshold	$V_{UVLO,UP}$				3	V
V_{CC} UVLO Hysteresis	$V_{UVLO,HYS}$			0.4		V
Quiescent Current	I_Q	V_{FB} = 1.3V		380		μA
Shutdown Current	I_S	V_{CC} = 5V, V_{EN} = 0V		1		μA
NFET $R_{DS(ON)}$	$R_{DS(ON)}$			65		mΩ
Maximum Peak Current Limit	I_{SM}	R_{ISET} = 75kΩ	8	9		A
Off-Time	t_{OFF}	R_{ADJ} = 200kΩ	1.75	2.0	3.25	μs
EN Rising Threshold	V_{ENH}		2.7			V
EN Falling Threshold	V_{ENL}				0.8	V
Minimum On-Time	$t_{ON,MIN}$			100		ns
Feedback Voltage	V_{FB}		1.225	1.25	1.275	V
FB Input Current	I_{FB}	V_{FB} = 3V	-50		50	nA
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Recovery Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

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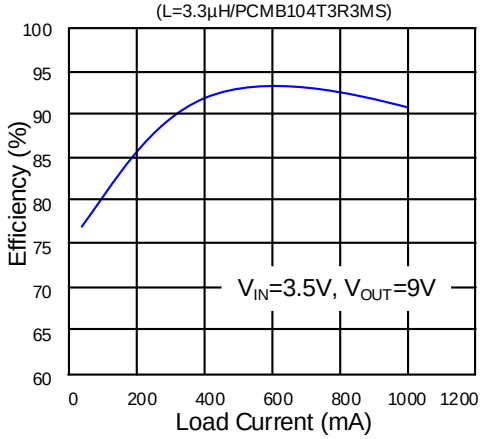
Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 3.5V, V_{OUT} = 9V, L = 3.3µH, C_{OUT} = 44µF, unless otherwise specified)

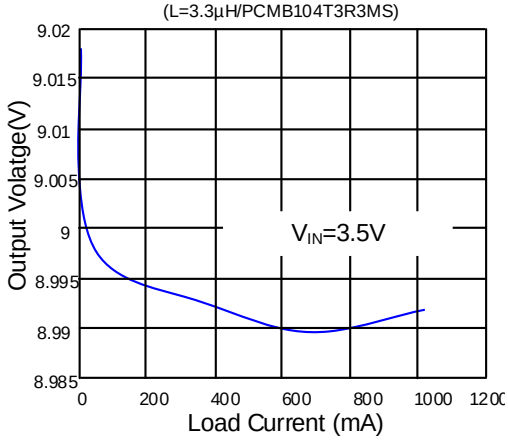
Efficiency vs. Load Current

(L=3.3µH/PCMB104T3R3MS)



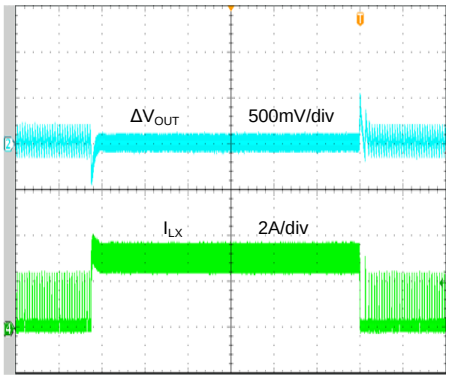
Load Regulation

(L=3.3µH/PCMB104T3R3MS)



Load Transient

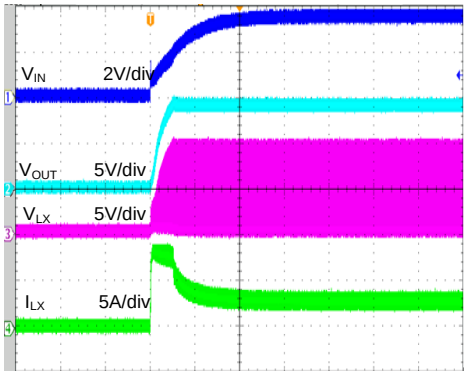
(V_{IN}=3.5V, V_{OUT}=9V,I_{OUT}=0.1~1A)



Time(800µs/div)

Startup from V_{IN}

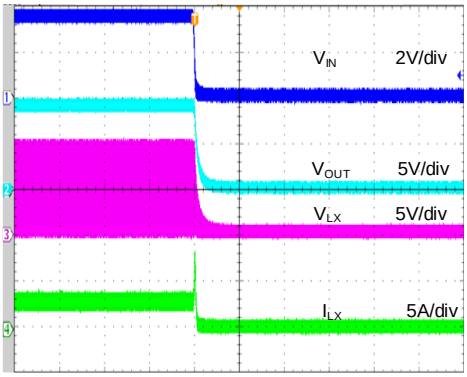
(V_{IN}=3.5V, V_{OUT}=9V,I_{OUT}=1A)



Time(4ms/div)

Shutdown from V_{IN}

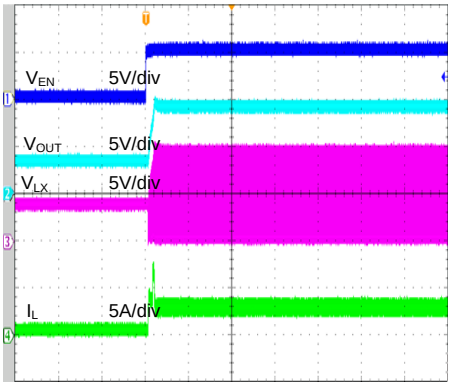
(V_{IN}=3.5V, V_{OUT}=9V,I_{OUT}=1A)



Time(4ms/div)

EN ON

(V_{IN}=3.5V, V_{OUT}=9V,I_{OUT}=1A)



Time(800us/div)

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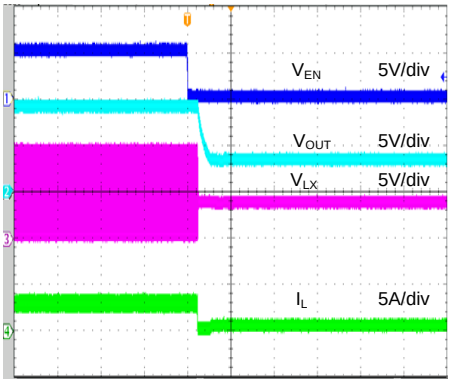
EN OFF

(V_{IN}=3.5V, V_{OUT}=9V,I_{OUT}=1A)



Time(800us/div)

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Detailed Description

The SY21299 high efficiency step-up regulator operates using current mode control over an input voltage range from 3V to 5.5V. It integrates an N-channel MOSFET with low 65mΩ $R_{DS(ON)}$ to minimize conduction loss. Built-in internal soft-start circuitry minimizes inrush current at startup.

Operation

The SY21299 operates using constant off-time peak current control. The one-shot circuit or on-time generator, which determines how long to turn off the low side power switch, is fundamental to any constant on-time (COT) architecture. Each off-time (t_{OFF}) is a programmable period that can be programmed by adjusting an external resistor.

The low side FET is turned on at the start of every switching cycle, and inductor current ramps up. After inductor current sampling voltage reaches the peak limit V_{COMP}, which is generated by FB, ref, and external components of COMP, an internal signal sets and the low side FET closes for a period of t_{OFF}. After remaining off for t_{OFF}, the low side FET turns on and starts a new period.

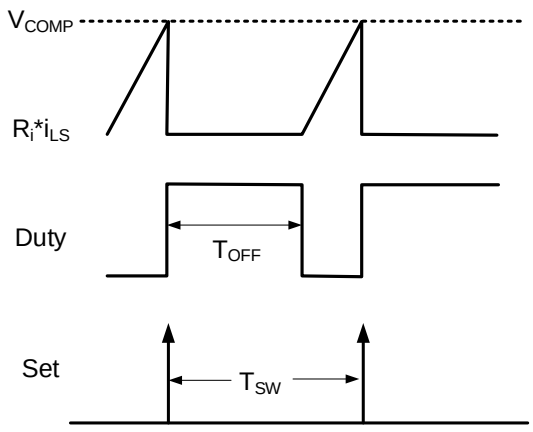


Figure 3. Constant On-Time Valley Current Control

Enable Operation

Driving the EN pin high (>2.7V) enables normal operation. Driving the EN pin low (<0.8V) places the device in shutdown mode. During shutdown, the SY21299 current drops to less than 1μA.

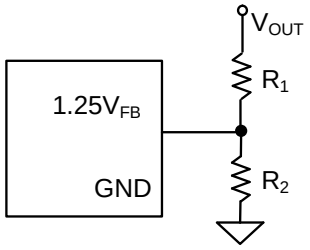
Application Information

The following paragraphs describe the selection process for the feedback resistors (R1 and R2), input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and diode D.

Feedback Resistor Divider R1 and R2

Choose R1 and R2 to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both R1 and R2 to minimize power consumption under light loads. If R1 is chosen, R2 can be calculated as:

$$R2 = \frac{R1 \times 1.25V}{V_{OUT} - 1.25V}$$



Current Limit Setting Resistor R_{ISET}

The current limit can be programmed by using an external resistor R_{ISET} connected to I_{SET} using the following equation:

$$R_{ISET} = \frac{680A}{I_{SM}} \times k\Omega$$

Programmable Constant Off-Time

The off-time can be programmed by using an external resistor R_{ADJ} connected to ADJ pin using the following equation:

$$R_{ADJ} = \frac{t_{OFF}}{10ns} \times k\Omega$$

Soft-start Circuit

The SY21299 has a built-in soft-start to control the rising slew rate of the output voltage and limit the input current surge during IC startup. For normal condition, the typical soft-start time is about 1ms. The higher output, larger capacitance and output current are used on the output, the soft-start time will proportionally increase.

Input Capacitor C_{IN}:

The ripple current through input capacitor C_{IN} is calculated as:

$$I_{CIN_RMS} = \frac{(V_{OUT} - V_{IN}) \times t_{OFF}}{2\sqrt{3} \times L}$$

Place a X5R or better grade ceramic capacitor as close as possible to the L1 and GND pins. Minimize the loop area

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formed by pins C_{IN}, L1, and GND. A 10µF low ESR ceramic capacitor is recommended for most applications.

V_{CC} Capacitor C_{VCC}:
The V_{CC} capacitor must be close to the V_{CC} and GND pins. Minimize the loop area formed by pins C_{VCC}, and V_{CC}/GND. A 2µF low ESR ceramic is recommended for most applications.

Output Capacitor C_{OUT}:
Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use two X5R or better grade ceramic capacitors with 35V rating, and capacitance greater than 10µF each.

Boost Inductor L
Consider the following when choosing this inductor:

- Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{IN}}{V_{OUT}} \times \frac{(V_{OUT} - V_{IN}) \times t_{OFF}}{I_{OUT,MAX} \times 40\%}$$

  where t_{OFF} is set by R_{ADJ} and $I_{OUT,MAX}$ is the maximum load current.

  The SY21299 can tolerate ripple current amplitude variations. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

- The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \frac{V_{OUT}}{V_{IN}} \times I_{OUT,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

- The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR less than 50mΩ to achieve good overall efficiency.

Rectifier Diode
For high efficiency, choose a Schottky diode with low forward voltage drop and fast reverse recovery. The maximum current rating of the diode must be higher than the maximum input current, and the average current rating of the diode must be higher than the output current.

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Loop Compensation

The SY21299 operates using constant off-time peak current control. The current-mode control scheme has two feedback loops:

- The inner loop (current loop) does not require any external compensation components.
- The outer loop (voltage loop) is compensated using external components.

In most applications, a Type 2 or Type 2a compensation network can be used to stabilize the voltage loop, as shown in Figure 4. Type 2 is the most widely used, and it works well for power stages lagging down to -90 degrees and in cases where the output capacitor ESR voltage must be canceled. Type 2a is used where the output capacitor ESR effect can be ignored.

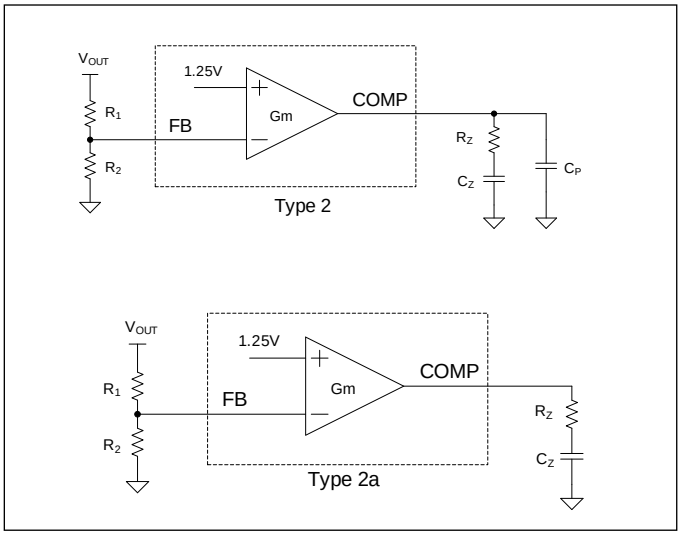

Figure 1. Compensation networks

Follow the steps below to calculate the value of external components for loop compensation.

1. Select the crossover frequency f_c of the closed loop.
   For the tradeoff of stability and transient response of the system, the recommend crossover frequency is the minimum value of 1/5 of right-half-plane zero (f_{RHPZ}) and 1/10 of the switching frequency. The system has a faster response at a higher crossover frequency.

$$f_{RHPZ} = \frac{(1-D_{MAX})^2 \times V_{OUT}}{2\pi \times L \times I_{OUT}}$$

2. Select an Rz value of the R-C series combination connected to the COMP pin.

$$R_Z = \frac{V_{OUT}}{g_m \times G_{fc} \times V_{REF}}$$

   where g_m is the error amplifier transconductance, which is typically 270μS; G_{fc} is the gain of the power stage at crossover frequency.

$$G_{fc} = \frac{(1-D_{MAX})}{2\pi \times fc \times C_{OUT} \times R_i}$$

   where R_i is the current sense gain, which is typically 150mΩ.

3. Select a Cz value of the R-C series combination connected to the COMP pin. The compensation zero decides phase margin at the crossover frequency. Place a compensation zero at or before the dominant pole of R_L and C_O. R_L is the load resistance, which equals V_{OUT}/I_{OUT}.

$$C_Z = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_Z}$$

4. A high frequency pole is recommended to attenuate the high frequency noise. Place this pole to cancel the ESR zero of C_{OUT}

$$C_P = \frac{R_{ESR} \times C_O}{R_Z}$$

Thermal protection

The SY21299 includes overtemperature protection circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. When the junction temperature cools down by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the thermal protection threshold.

Overcurrent Protection

The SY21299 provides cycle-by-cycle peak current protection and turns off the main power MOSFET once the inductor current reaches the current limit threshold. During the overcurrent protection, the output voltage drops as a function of the load. As soon as the overload condition is removed, the converter resumes operation.

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Maximum Output Current Estimation

The maximum current that the converter can provide to the load depends on the output voltage / input voltage ratio and the programmed current limit.

Use the following equations to evaluate an approximate max current that the converter can deliver when driving the load.

$$D=1-V_{IN(MIN)}\times\frac{\eta}{V_{OUT}}$$

Estimate the maximum output current:

$$I_{MAXOUT}=(IL_{MIN}-\frac{\Delta IL}{2})\times\frac{\eta\times V_{IN(MIN)}}{V_{OUT}}$$

$$I_{MAXOUT}=\left(I_{LIM(MIN)}-\frac{\Delta IL}{2}\right)\times(1-D)$$

Where: $V_{IN(MIN)}$ is the minimum voltage at the boost input in the application, IL_{MIN} is the minimum programmed current limit, ΔIL is the current ripple and η is the efficiency, which can be substituted with a value of 0.8 for simplicity.

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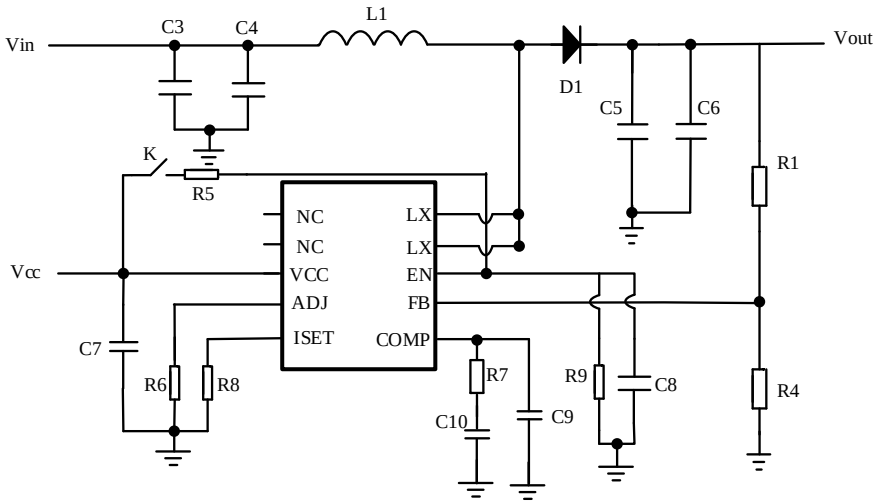
Application Schematic



Design Specifications

Input Voltage (V)	Output Voltage(V)	Input Current (A)
3-5	9	1

BOM List

Reference Designator	Description	Part Number	Manufacturer
C1	220μF/50V (electronic capacitor)		
C3,C4	2.2μF/50V,1206,X7R	C3216X7R1H225K	TDK
C5,C6	22μF/25V,1206,X5R	C3216X5R1E226M	TDK
C7	1μF/25V,0603,X7R	C1608X7R1E105K	TDK
C8	100nF/50V,0603,X7R	C1608X7R1H104K	TDK
C9	22pF/50V,0603	C1608C0G1H220J	TDK
C10	1nF/50V,0603	C1608C0G1H102J	TDK
R1	100kΩ,1%,0603		
R4	16.1kΩ,1%,0603		
R5	1kΩ,1%,0603		
R6	51kΩ,1%,0603		
R7	49.9kΩ,1%,0603		
R8	82kΩ,1%,0603		
R9	1MΩ,1%,0603		
R10	10Ω,1%,0603		
D1	40V 5A Schottky, SMB	SS54	
L1	3.3μH/10A	PCMB104T3R3MS	CYNTECCO.,LTD

Recommended Components for Typical Applications

V_{OUT}(V)	R1(kΩ)	R2(kΩ)	L(μH)	C3
9	100	16.1	3.3	2×22μF/25V/X7R,1206

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Layout Design

To achieve optimal design, follow these PCB layout considerations:

- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if cost allows.
- C_{OUT} must be close to D1 and pins LX and GND. Minimize the loop area formed by C_{OUT}, and GND.
- To reduce the switching noise, minimize the PCB copper area connected to the LX pin.
- In order to reduce crosstalk, RFBH, RFBL, and the trace connected to the FB pin must not be adjacent to the LX net on the PCB layout.
- The VCC capacitor must be close to the VCC and GND pins

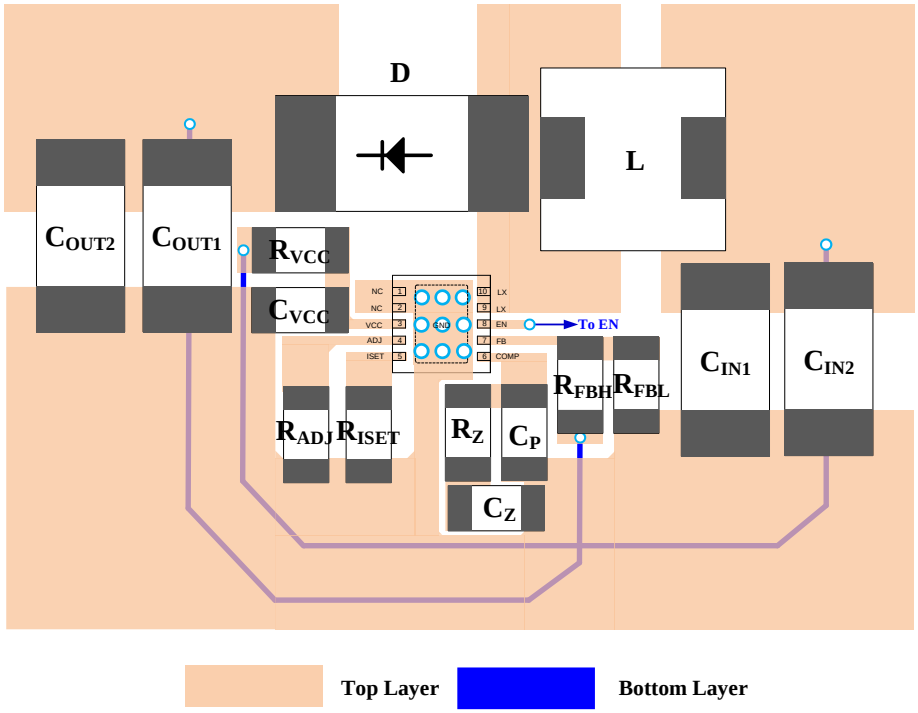

Figure 5. Suggested PCB Layout

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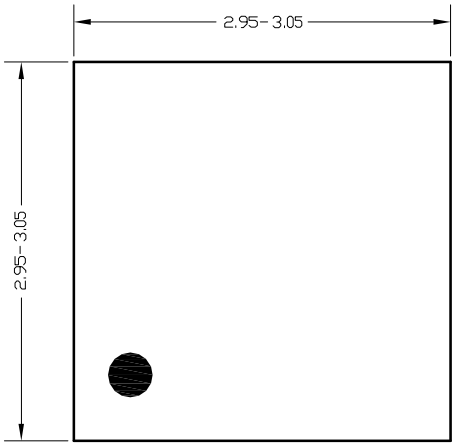
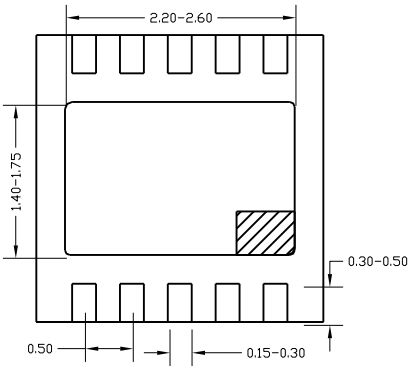
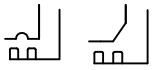
DFN3x3-10 Package Outline and PCB Layout



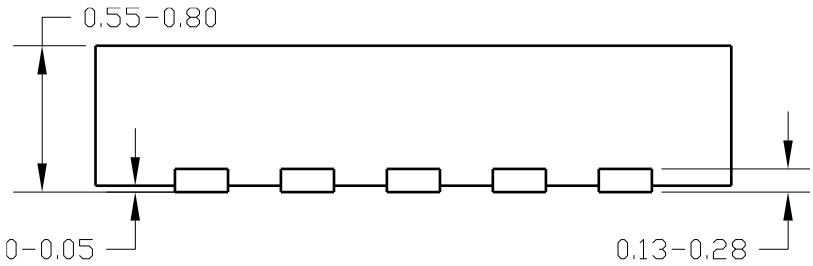
Top view



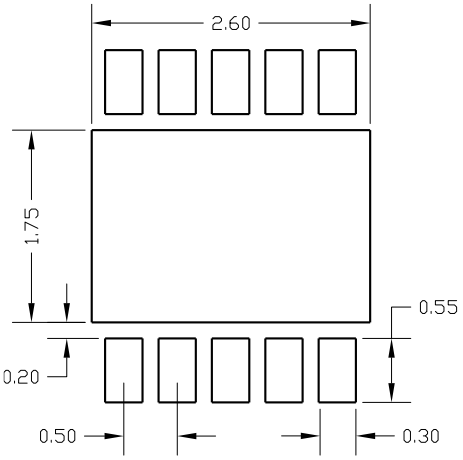
Bottom view



Detail A
Pin1 identifier: two options



Side view



Recommended pad layout
(reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

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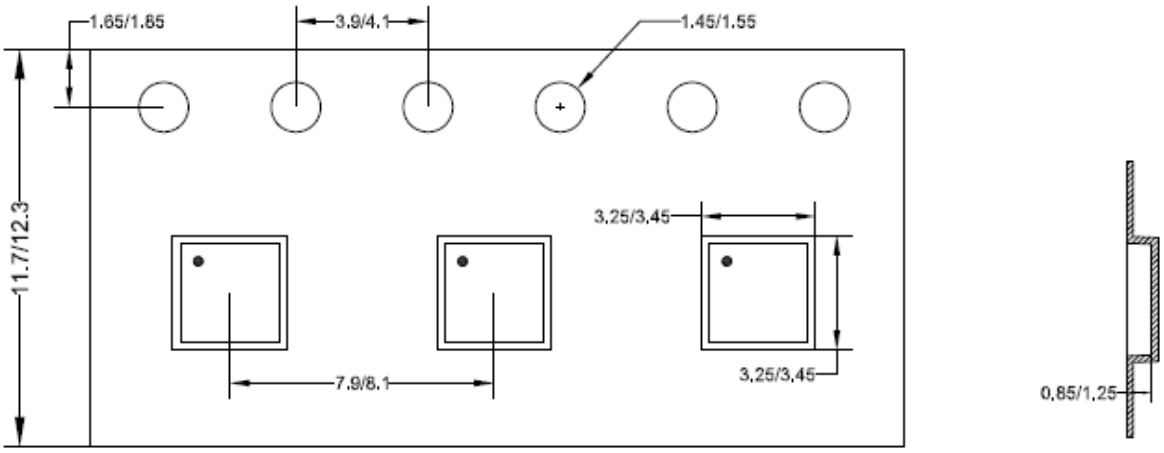
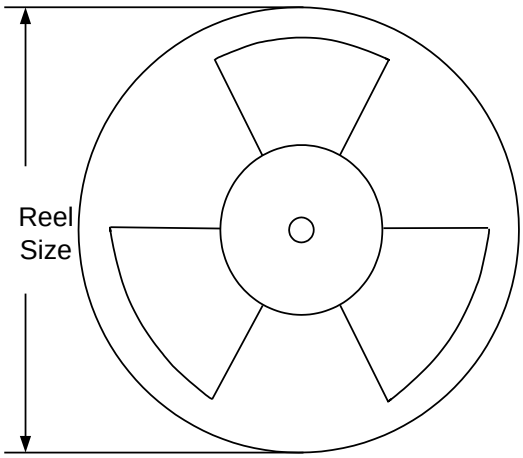
Taping and Reel Specification

DFN3×3 taping orientation



Feeding direction →

Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3x3	**12**	**8**	**13"**	**400**	**400**	**5000**

Others: NA

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Oct.12, 2023	Revision 1.0	Language improvements for clarity.
Nov.25, 2014	Revision 0.9	Initial Release

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