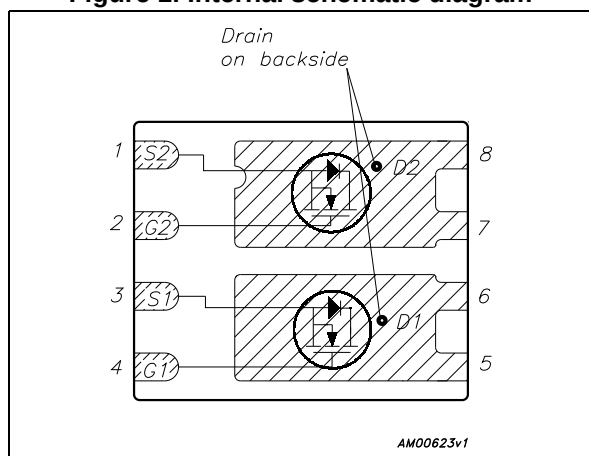


Automotive-grade dual N-channel 30 V, 0.016 Ω typ., 40 A STripFET™ H5 Power MOSFET in PowerFLAT™ 5x6 double island

Datasheet - production data



Figure 1. Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STL40DN3LLH5	30 V	0.018 Ω	40 A

- Designed for automotive application and AEC-Q101 qualified
- Low on-resistance
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™ H5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1. Device summary

Order code	Marking	Package	Packing
STL40DN3LLH5	40DN3LLH5	PowerFLAT™ 5x6 double island	Tape and reel

Contents

1 **Electrical ratings** 3

2 **Electrical characteristics** 4

 2.1 Electrical characteristics (curves) 6

3 **Test circuits** 8

4 **Package information** 9

 4.1 PowerFLAT 5x6 double island WF type R 10

5 **Packing information** 13

6 **Revision history** 15



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 22	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	40	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	28	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25^\circ\text{C}$	11	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb}=100^\circ\text{C}$	7	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	44	A
$I_{DM}^{(1)(3)}$	Drain current (pulsed)	160	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	50	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25^\circ\text{C}$	4.7	W
T_J	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

1. The value is rated according R_{thj-c}
2. The value is rated according $R_{thj-pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	3.0	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	32	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

($T_{CASE}=25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}^{(1)}$			10	μA
I_{GSS}	Gate body leakage current	$V_{GS} = \pm 22\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1	1.5		V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 5.5\text{ A}$		0.016	0.018	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 5.5\text{ A}$		0.02	0.025	Ω

1. Defined by design, not subject to production test

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	475	-	pF
C_{oss}	Output capacitance		-	97	-	pF
C_{rss}	Reverse transfer capacitance		-	19	-	pF
Q_g	Total gate charge	$V_{DD} = 15\text{ V}$, $I_D = 11\text{ A}$ $V_{GS} = 4.5\text{ V}$ (see Figure 13)	-	4.5	-	nC
Q_{gs}	Gate-source charge		-	1.7	-	nC
Q_{gd}	Gate-drain charge		-	1.9	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$, $I_D = 11\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 12)	-	4	-	ns
t_r	Rise time		-	22	-	ns
$t_{d(off)}$	Turn-off delay time		-	13	-	ns
t_f	Fall time		-	2.8	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 11\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 25\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$	-	16.2		ns
Q_{rr}	Reverse recovery charge		-	1		nC
I_{RRM}	Reverse recovery current		-	8.1		A

1. Pulsed: pulse duration=300 μ s, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

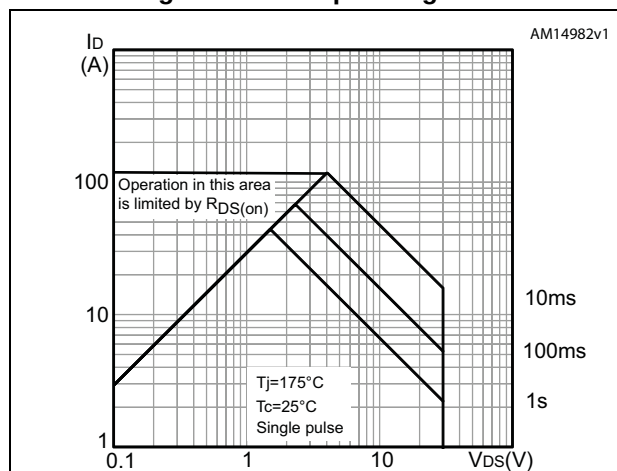


Figure 3. Thermal impedance

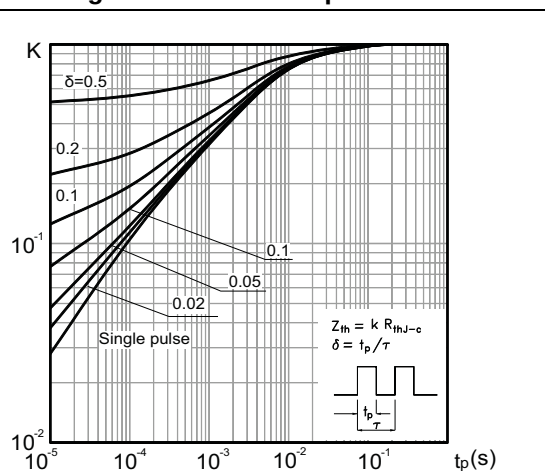


Figure 4. Output characteristics

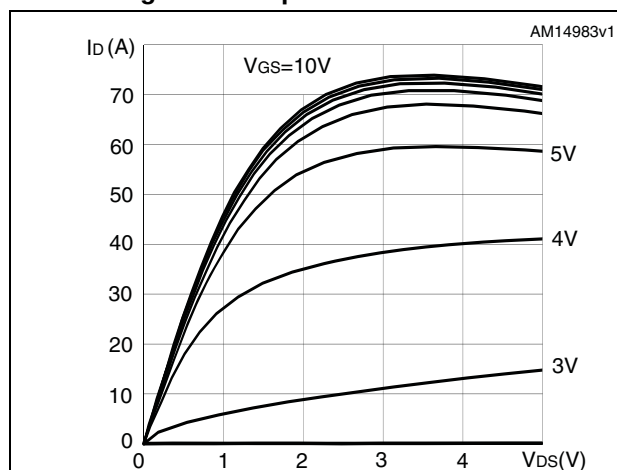


Figure 5. Transfer characteristics

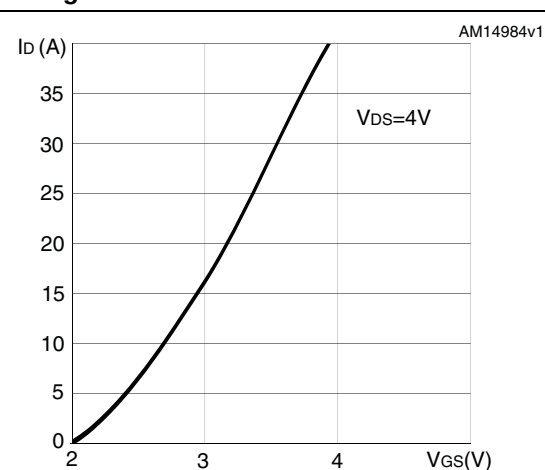
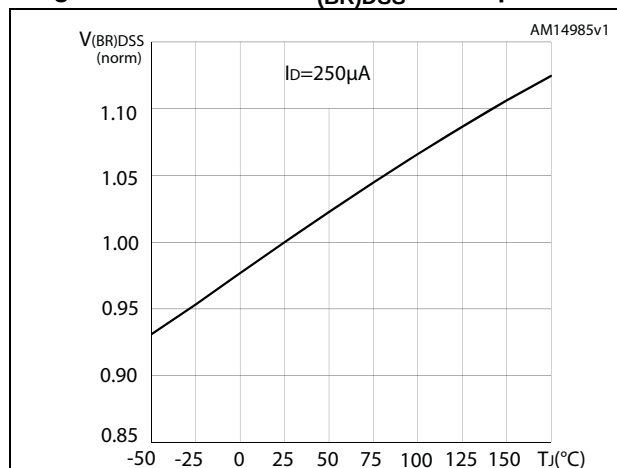
Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

Figure 7. Static drain-source on-resistance

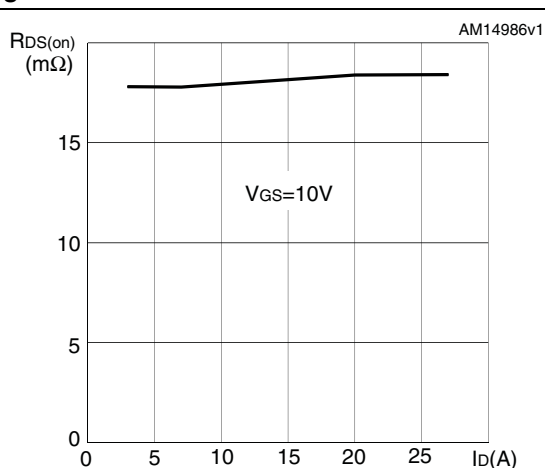


Figure 8. Gate charge vs gate-source voltage

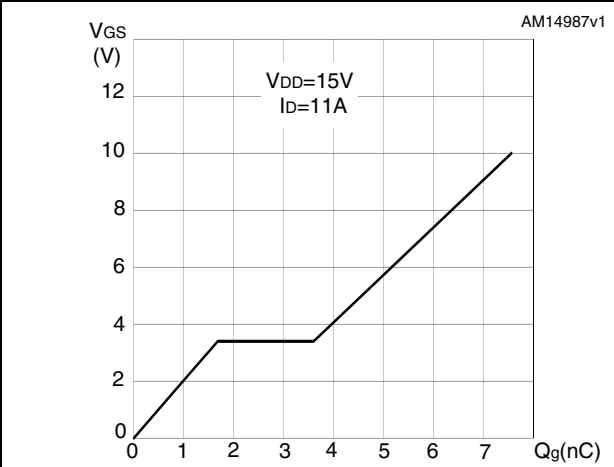


Figure 9. Capacitance variations

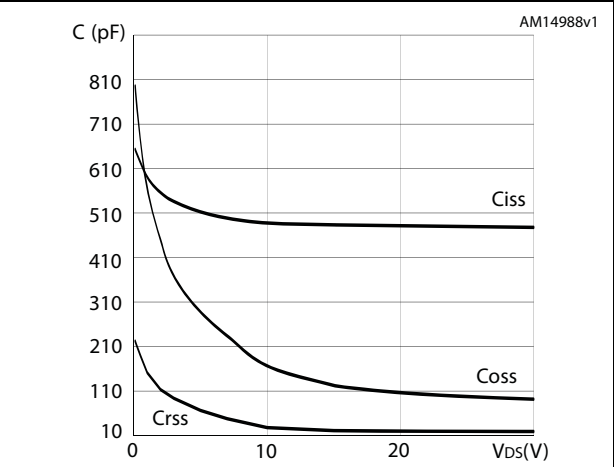


Figure 10. Normalized gate threshold voltage vs temperature

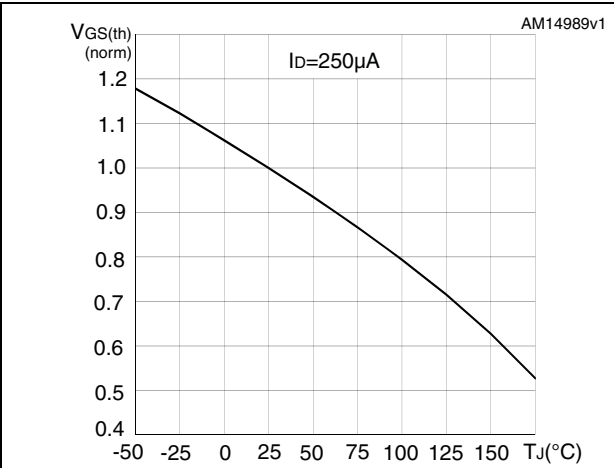
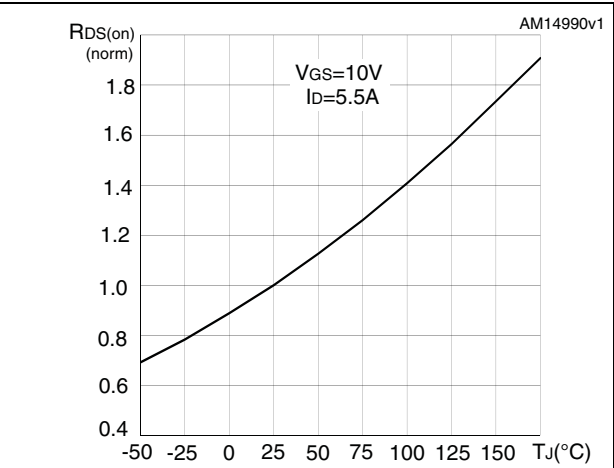


Figure 11. Normalized on-resistance vs temperature



3 Test circuits

Figure 12. Switching times test circuit for resistive load

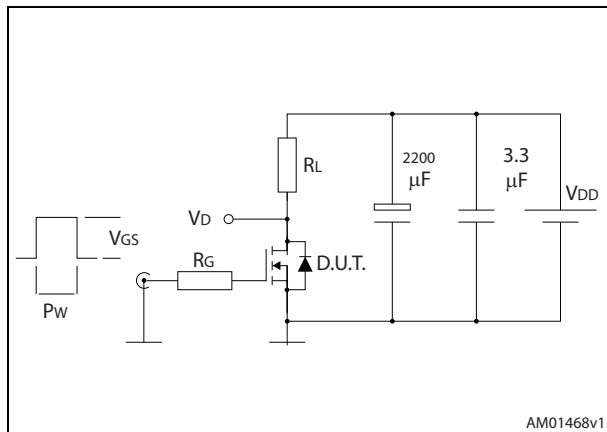


Figure 13. Gate charge test circuit

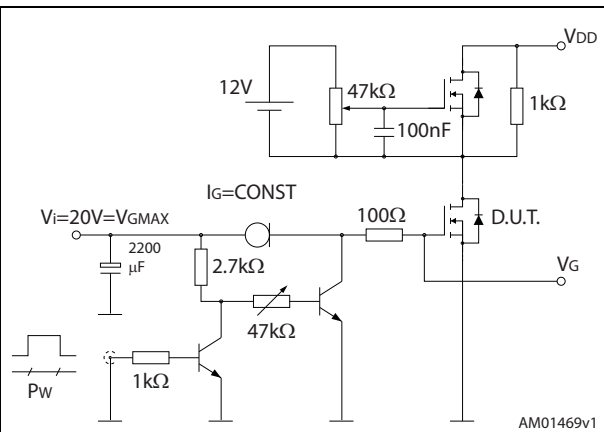


Figure 14. Test circuit for inductive load switching and diode recovery times

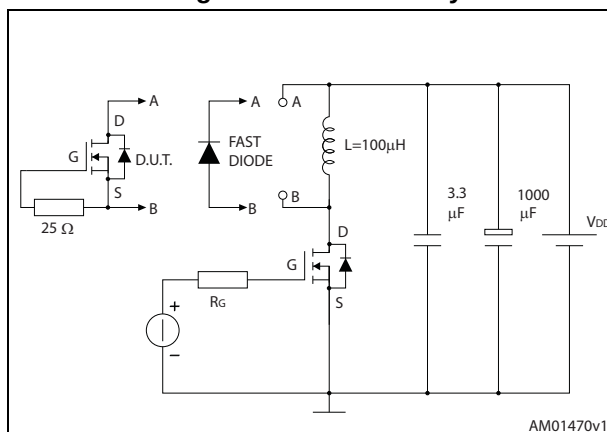


Figure 15. Unclamped inductive load test circuit

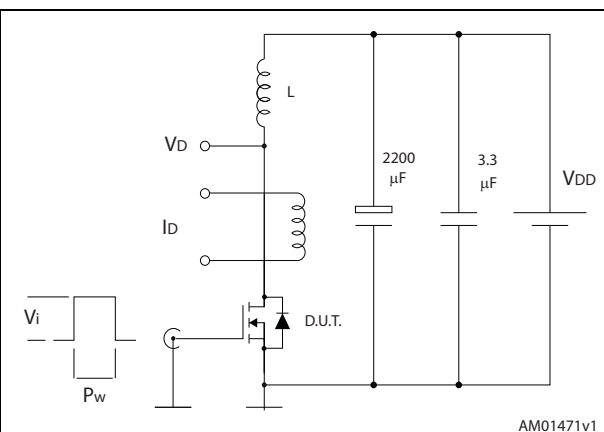


Figure 16. Unclamped inductive waveform

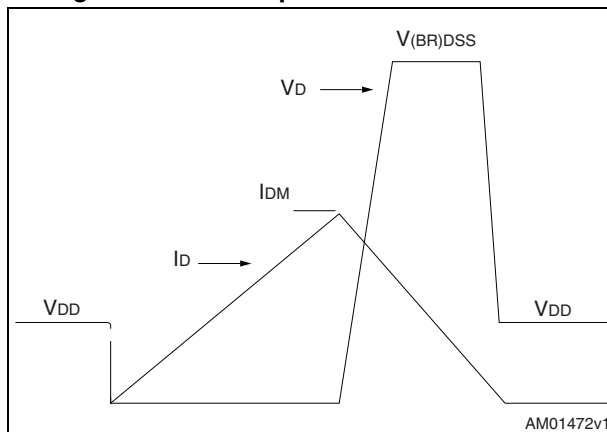
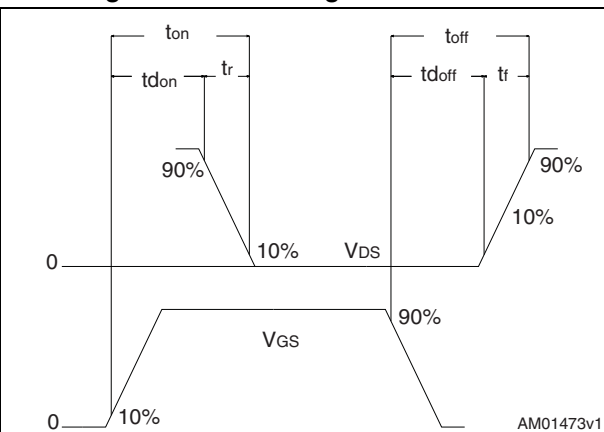


Figure 17. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 PowerFLAT 5x6 double island WF type R

Figure 18. PowerFLAT 5x6 double island WF type R outline

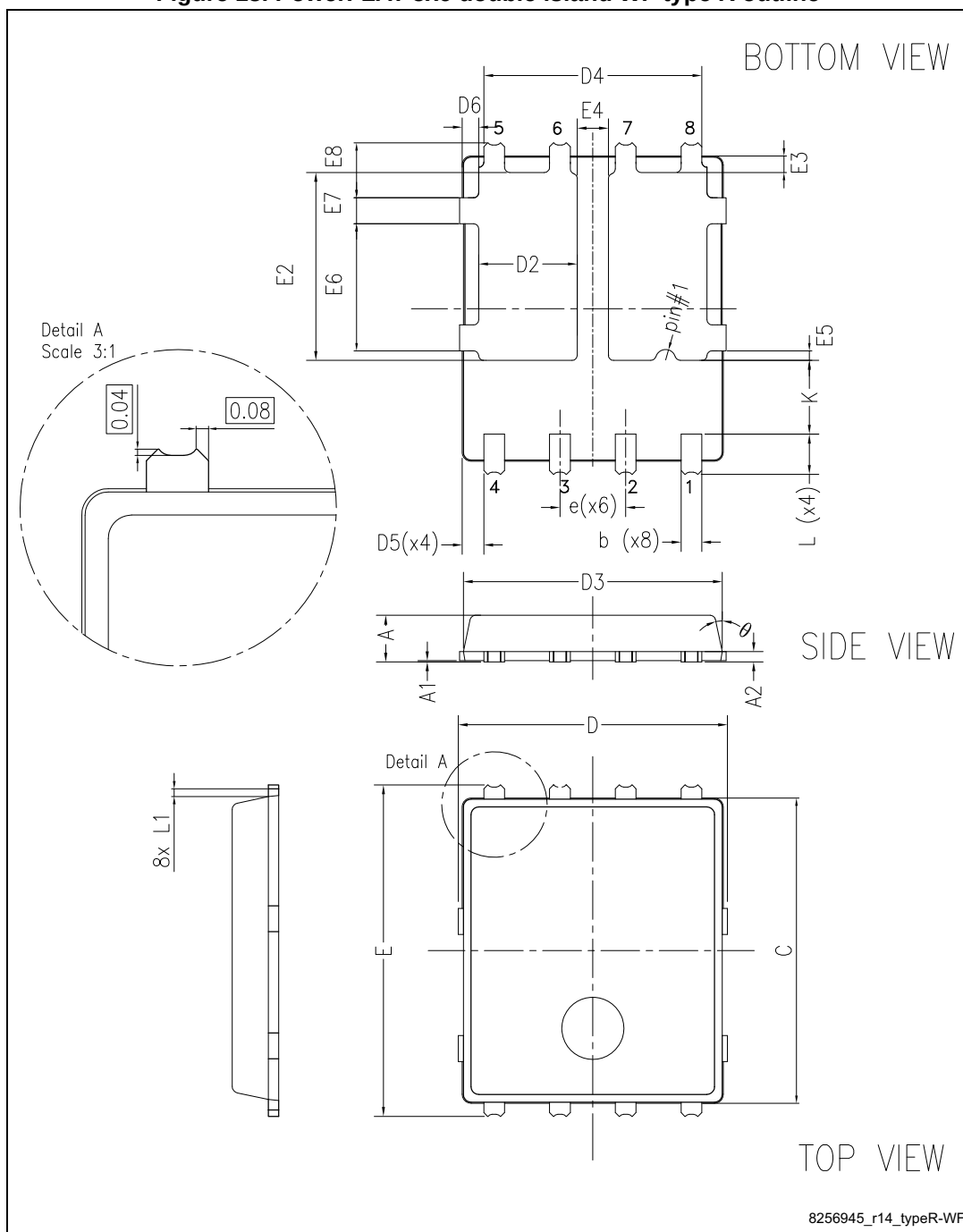
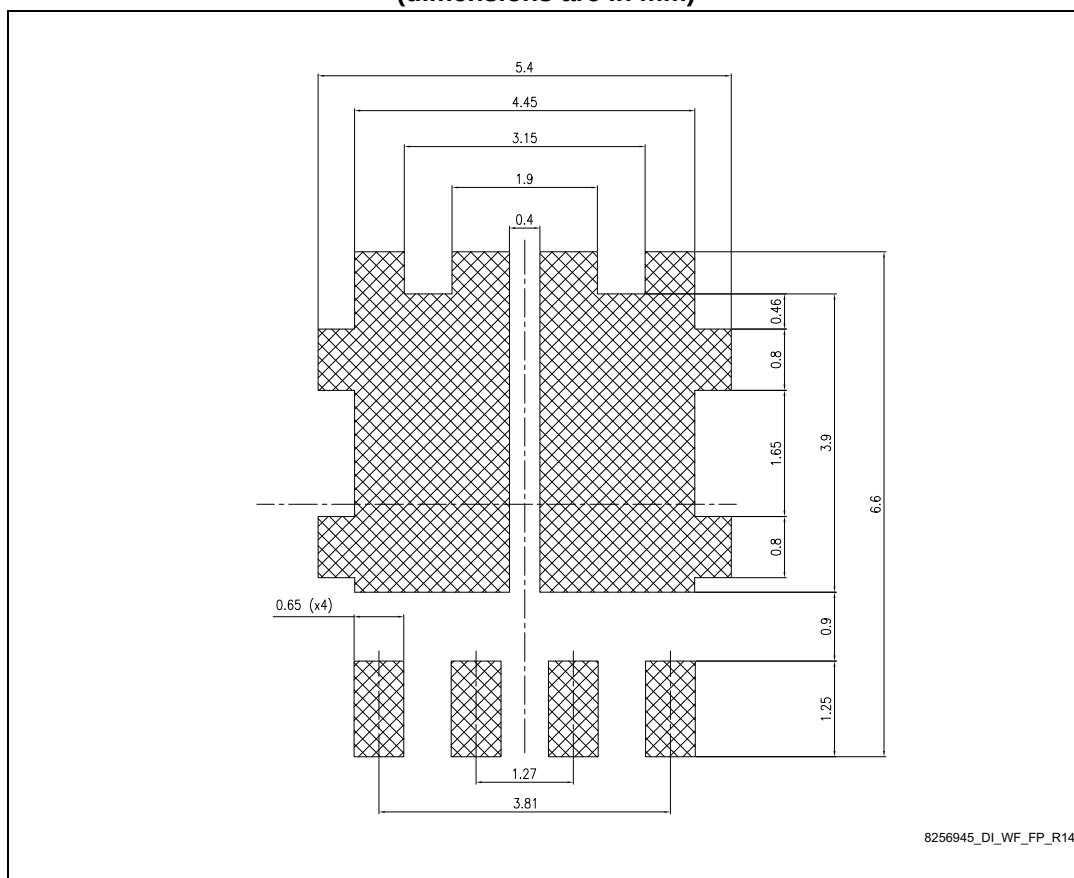


Table 8. PowerFLAT 5x6 double island WF type R mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	1.68		1.88
D3	4.80	5.00	5.20
D4	4.05	4.20	4.35
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E4	0.55		0.75
E6	2.35		2.55
E7	0.40		0.60
K	1.275		1.575
L	0.70		0.90
L1		0.275	
θ	0°		12°

**Figure 19. PowerFLAT™ 5x6 double island recommended footprint
(dimensions are in mm)**



5 Packing information

Figure 20. PowerFLAT™ 5x6 WF tape

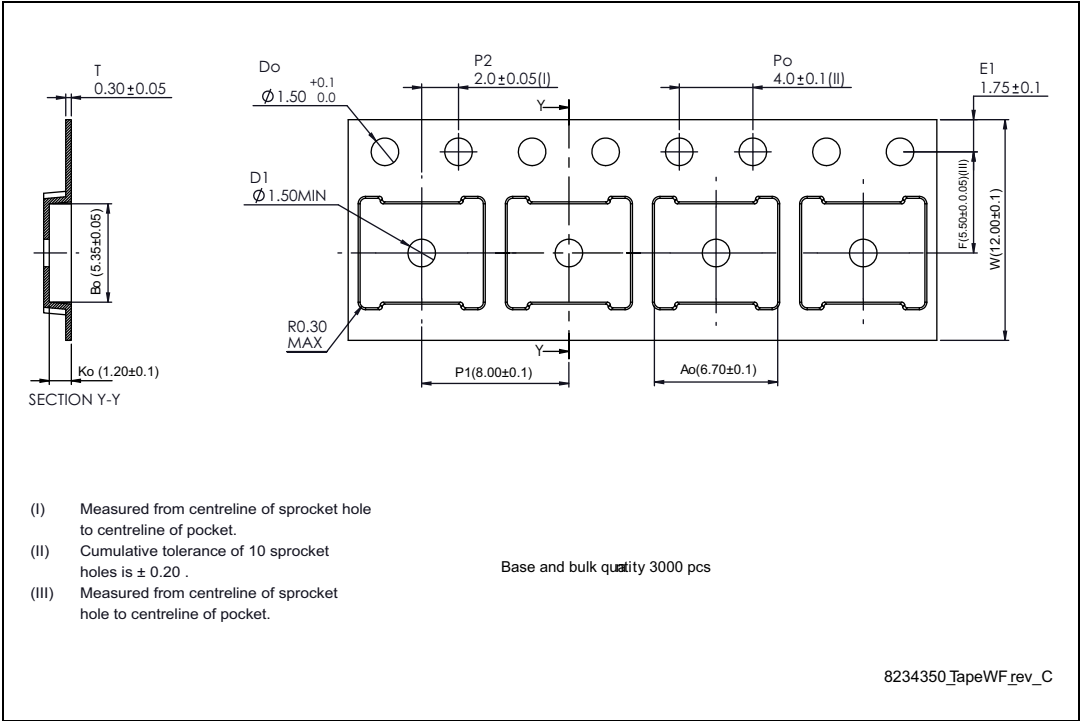


Figure 21. PowerFLAT™ 5x6 package orientation in carrier tape

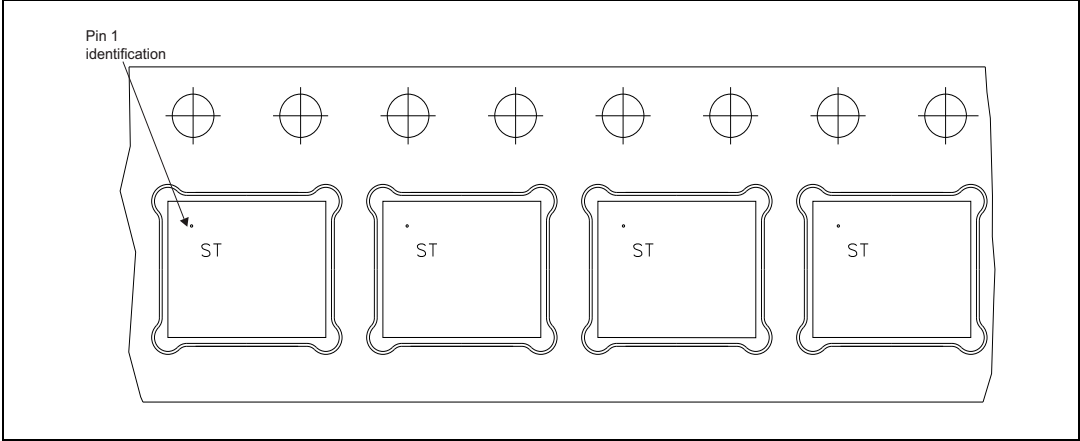
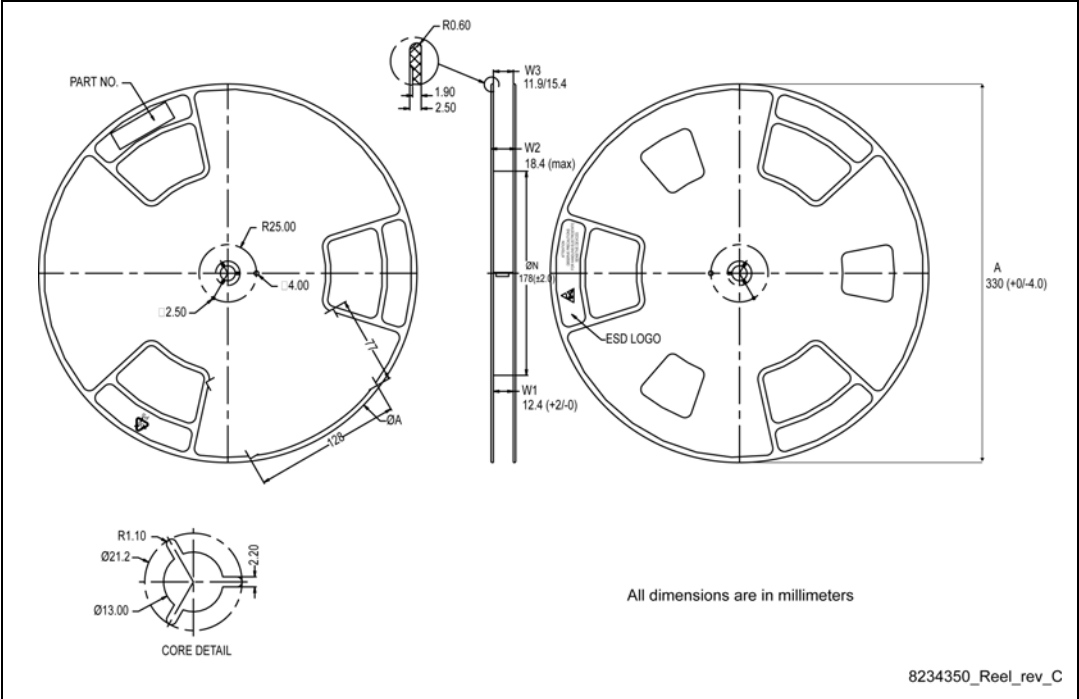


Figure 22. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
24-Jan-2011	1	First release.
03-Oct-2012	2	Section 2.1: Electrical characteristics (curves) has been added. Document status promoted from preliminary data to datasheet. Minor text changes.
14-Dec-2012	3	Modified the Applications section on the coverpage to "Automotive switching applications".
23-Feb-2015	4	Updated Section 4: Package mechanical data and added Section 5: Packing information. Updated title and features in cover page. Minor text changes.
27-Oct-2015	5	Updated title and features in cover page. Updated Table 2, Table 3, Table 4 and Table 7. Updated Section 4: Package information Minor text changes.
11-Mar-2016	6	Updated silhouette in cover page. Updated Table 1: Device summary , Table 2: Absolute maximum ratings , Table 3: Thermal resistance and Table 4: On/off states . Updated Figure 2: Safe operating area . Updated Section 4.1: PowerFLAT 5x6 double island WF type R Updated Section 5: Packing information . Minor text changes.

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