



PJA3471

100V P-Channel Enhancement Mode MOSFET

Voltage **-100 V**

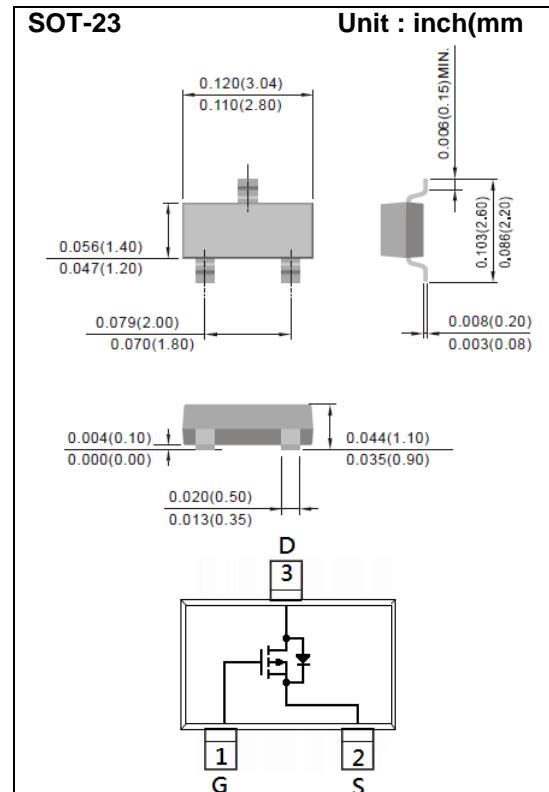
Current **-0.9 A**

Features

- $R_{DS(ON)}$, $VGS@-10V$, $I_D@-0.9A<650m\Omega$
- $R_{DS(ON)}$, $VGS@-4.5V$, $I_D@-0.45A<700m\Omega$
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : SOT-23 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0003 ounces, 0. 0084 grams



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current (^{Note 4})	I_D	-0.9	A
$T_A=70^\circ C$		-0.75	
Pulsed Drain Current (^{Note 1})	I_{DM}	-3.6	
Power Dissipation	P_D	1.25	W
$T_A=25^\circ C$		0.8	
Single Pulse Avalanche Energy (^{Note 6})	E_{AS}	0.2	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	°C
Typical Thermal resistance - Junction to Ambient (^{Note 4,5})	$R_{\theta JA}$	100	°C/W



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-100	-	-	V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-1	-2	-2.5	
Drain-Source On-State Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=-10\text{V}, I_{\text{D}}=-0.9\text{A}$	-	500	650	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}, I_{\text{D}}=-0.45\text{A}$	-	560	700	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=-80\text{V}, V_{\text{GS}}=0\text{V}$	-	-	-1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Dynamic (Note 7)						
Total Gate Charge	Q_g	$V_{\text{DS}}=-50\text{V}, I_{\text{D}}=-1\text{A},$ $V_{\text{GS}}=-10\text{V}$ (Note 2,3)	-	8	-	nC
Gate-Source Charge	Q_{gs}		-	1.8	-	
Gate-Drain Charge	Q_{gd}		-	1.4	-	
Input Capacitance	C_{iss}	$V_{\text{DS}}=-15\text{V}, V_{\text{GS}}=0\text{V},$ $f=1\text{MHz}$	-	448	-	pF
Output Capacitance	C_{oss}		-	28	-	
Reverse Transfer Capacitance	C_{rss}		-	21	-	
Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DS}}=-50\text{V}, I_{\text{D}}=1\text{A},$ $V_{\text{GS}}=-10\text{V}, R_{\text{G}}=6.2\Omega$ (Note 2,3)	-	3.7	-	ns
Turn-On Rise Time	t_{r}		-	25	-	
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	21	-	
Turn-Off Fall Time	t_{f}		-	22	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_s	---	-	-	-1.5	A
Diode Forward Voltage	V_{SD}	$I_s=1\text{A}, V_{\text{GS}}=0\text{V}$	-	-0.82	-1.2	V

NOTES :

1. Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is package limited.
4. Repetitive rating, pulse width limited by junction temperature $T_{\text{J}(\text{MAX})}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_{\text{J}}=25^\circ\text{C}$.
5. The test condition is $L=0.1\text{mH}, I_{\text{AS}}=-2\text{A}, V_{\text{DD}}=-25\text{V}, V_{\text{GS}}=-10\text{V}$
6. R_{QJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
7. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

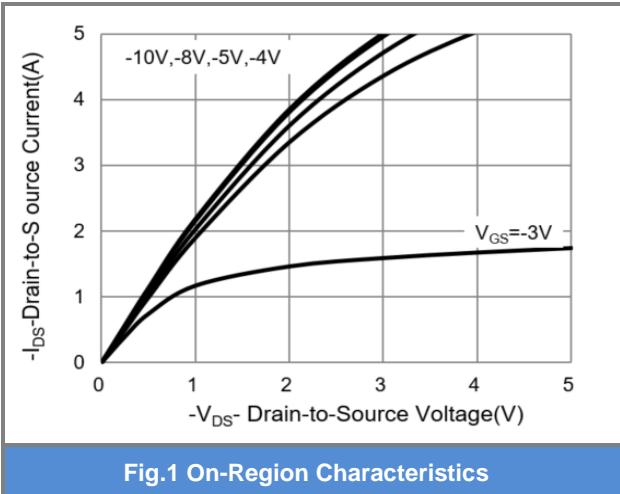


Fig.1 On-Region Characteristics

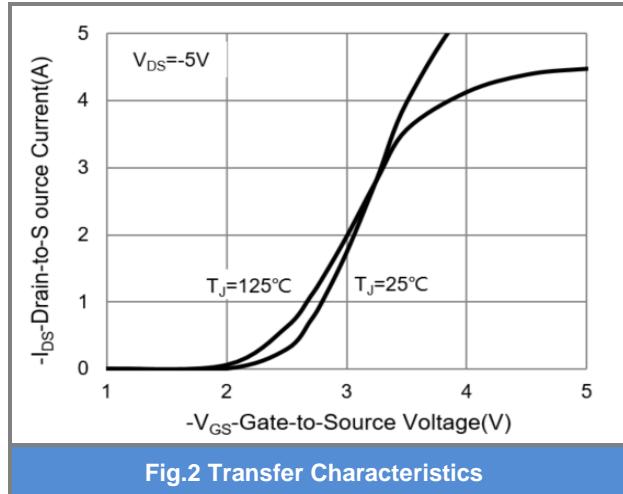


Fig.2 Transfer Characteristics

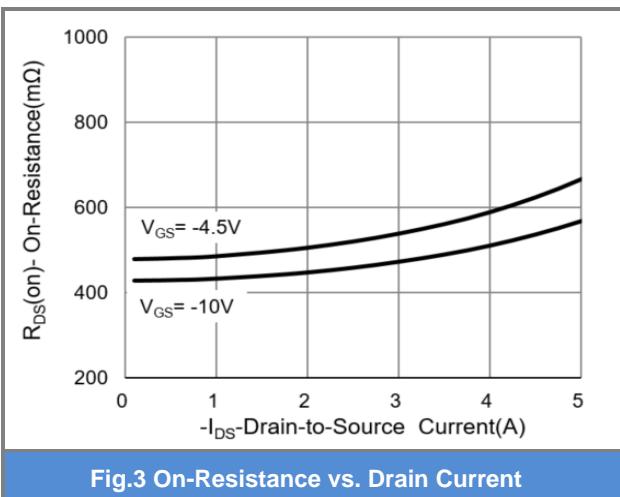


Fig.3 On-Resistance vs. Drain Current

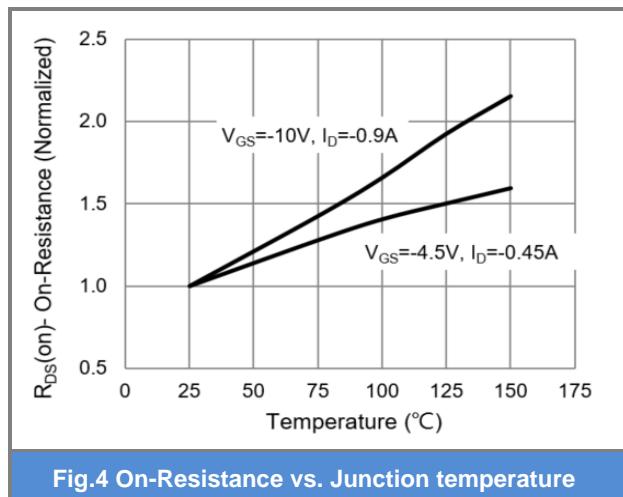


Fig.4 On-Resistance vs. Junction temperature

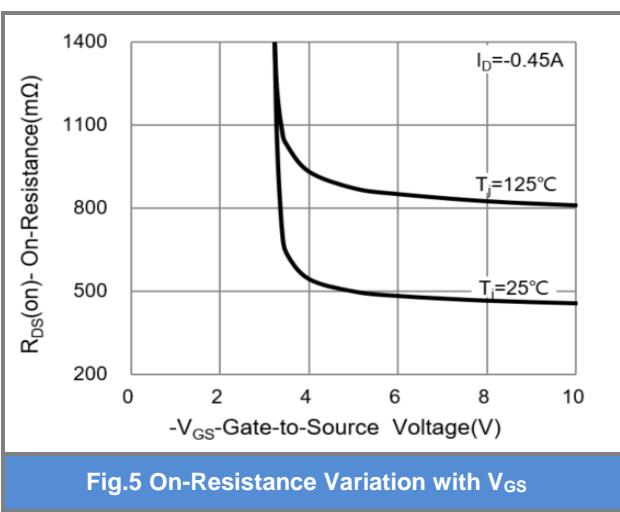


Fig.5 On-Resistance Variation with V_Gs

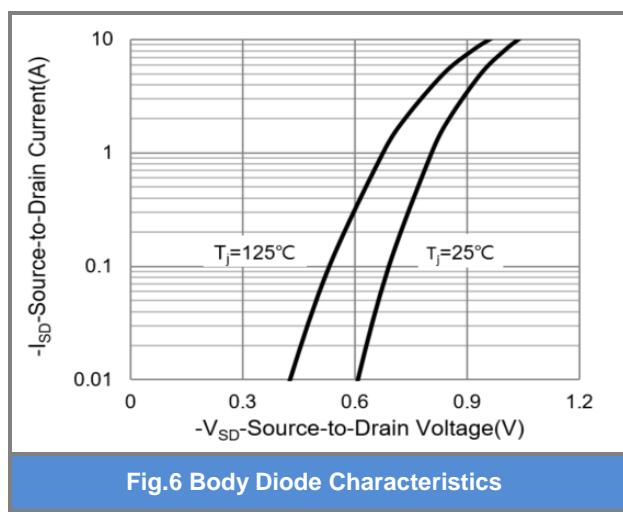


Fig.6 Body Diode Characteristics



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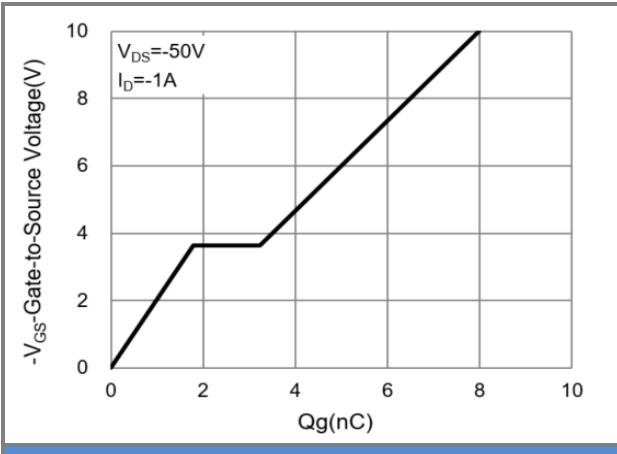


Fig.7 Gate-Charge Characteristics

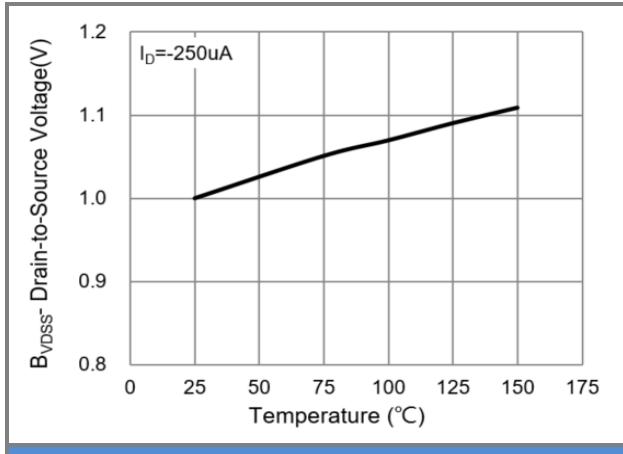


Fig.8 Breakdown Voltage Variation vs. Temperature

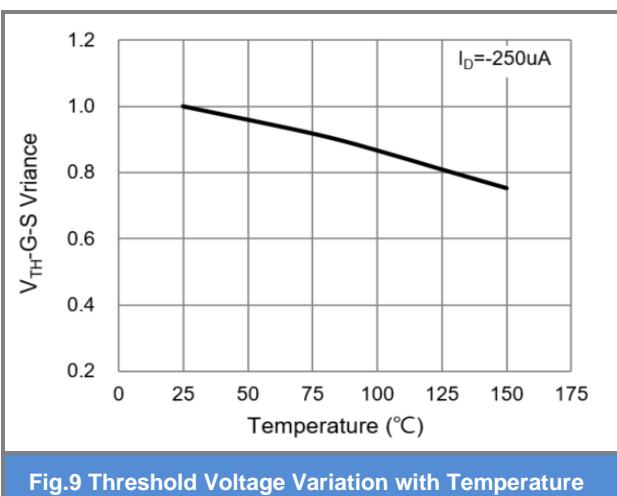


Fig.9 Threshold Voltage Variation with Temperature

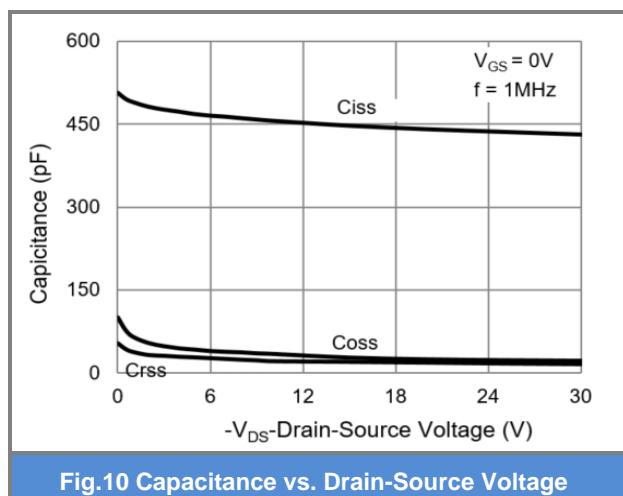


Fig.10 Capacitance vs. Drain-Source Voltage

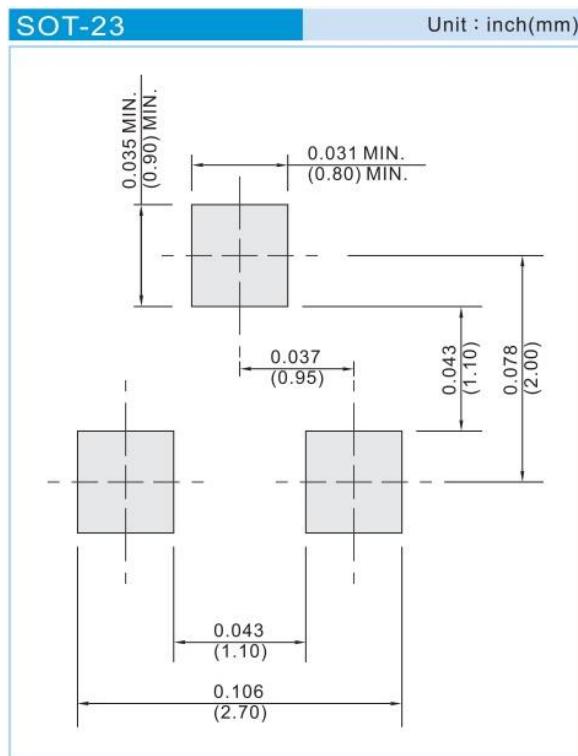


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Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJA3471_R1_00001	SOT-23	3K pcs / 7" reel	A71	Halogen free

Mounting Pad Layout





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