4.8V Bidirectional ESD and Surge Protection Device

NSPM3041

The NSPM3041 is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, high peak pulse current handling capability and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in cellular phones, tablets, MP3 players, digital cameras and many other portable applications where board space comes at a premium.

Features

- Low Clamping Voltage
- Low Leakage
- Small Body Outline: 1.0 mm x 0.6 mm
- Protection for the following IEC Standards:
  IEC61000−4−2 Level 4: ±30 kV Contact Discharge
  IEC61000−4−5 (Lightning) 40 A (8/20 μs)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery Line Protection
- Audio Line Protection
- GPIO

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
IEC 61000−4−2 (ESD)	Contact Air		±30 ±30	kV
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−65 to +150	°C
Maximum Peak Pulse Current		I_{PP}	40	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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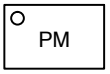
X2DFN2
CASE 714AB

MARKING DIAGRAM



P = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NSPM3041MXT5G	X2DFN2 (Pb−Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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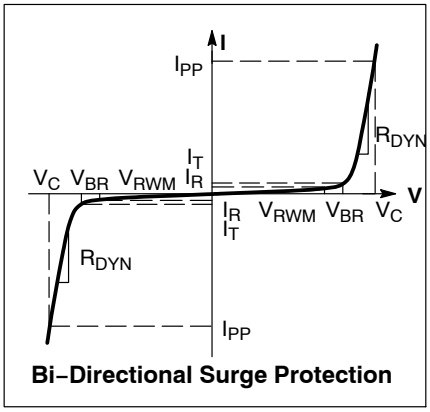
ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional Surge Protection

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			4.8	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	5.3	6.1	7.5	V
Reverse Leakage Current	I_R	V_{RWM} = 4.8 V, I/O Pin to GND			0.1	μA
Clamping Voltage	V_C	IEC61000−4−2, ±8 kV Contact	See Figures 1 & 2			V
Clamping Voltage TLP (Note 1)	V_C	I_{PP} = 8 A, IEC61000−4−2 Level 2 Equivalent (±4 kV Contact, ± 8 kV Air)		6.0		V
		I_{PP} = 16 A, IEC61000−4−2 Level 4 Equivalent (±8 kV Contact, ± 15 kV Air)		6.25		
Reverse Peak Pulse Current	I_{PP}	IEC61000−4−5 (8 x 20 μs) per Figure 14	40			A
Clamping Voltage 8x20 μs Waveform per Figure 14 (Note 2)	V_C	I_{PP} = 1 A I_{PP} = 40 A		5.6 7.8	6.6 8.5	V
Dynamic Resistance	R_{DYN}	100 ns TLP Pulse		0.03		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz		80	100	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. ANSI/ESD STM5.5.1 Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP condtions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 1 ns, averaging window: t_1 = 70 ns to t_2 = 90 ns.
2. Non−repetitive current pulse at T_A = 25°C, per IEC61000−4−5 waveform.

TYPICAL CHARACTERISTICS

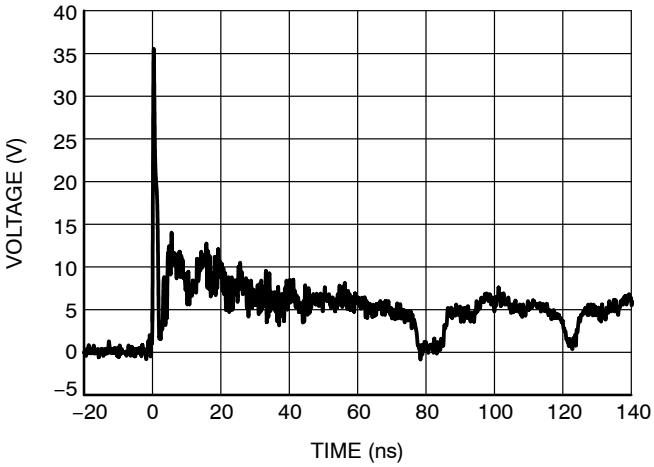


Figure 1. ESD Clamping Voltage Positive 8 kV Contact per IEC61000−4−2

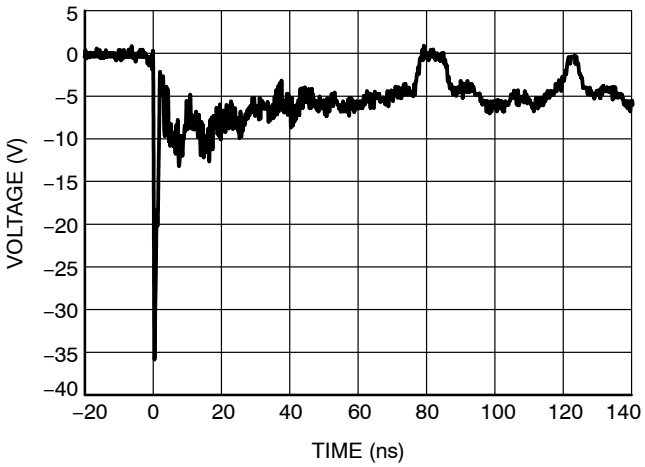


Figure 2. ESD Clamping Voltage Negative 8 kV Contact per IEC61000−4−2

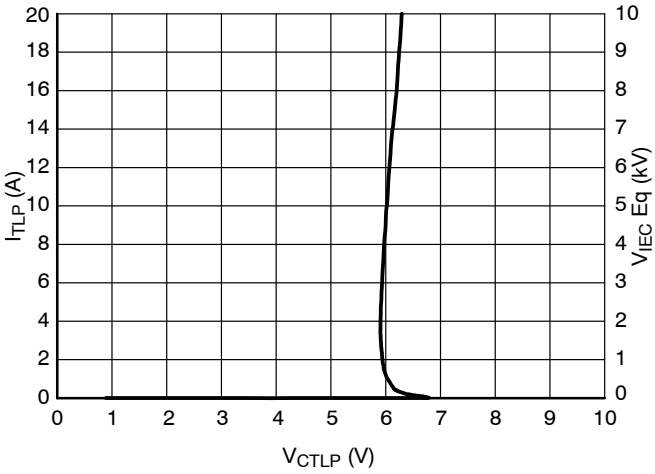


Figure 3. Positive TLP I−V Curve

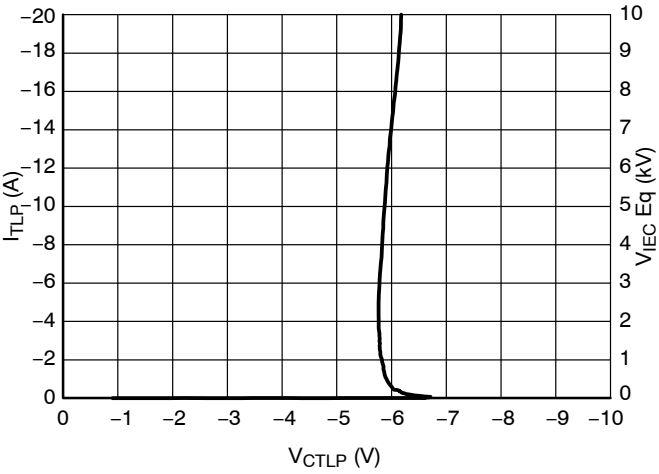


Figure 4. Negative TLP I−V Curve

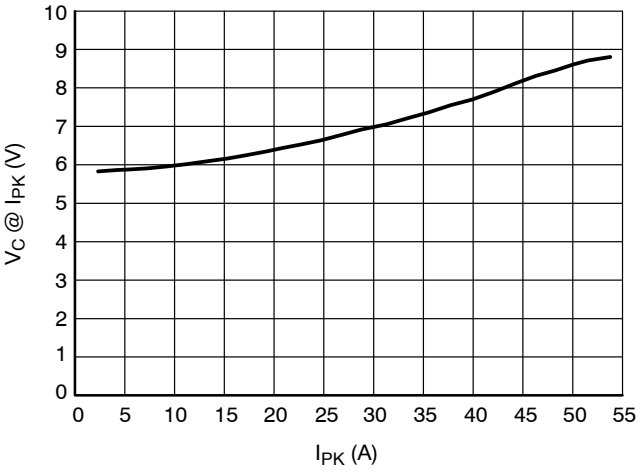


Figure 5. Positive Clamping Voltage vs. Peak Pulse Current (t_p = 8/20 μs)

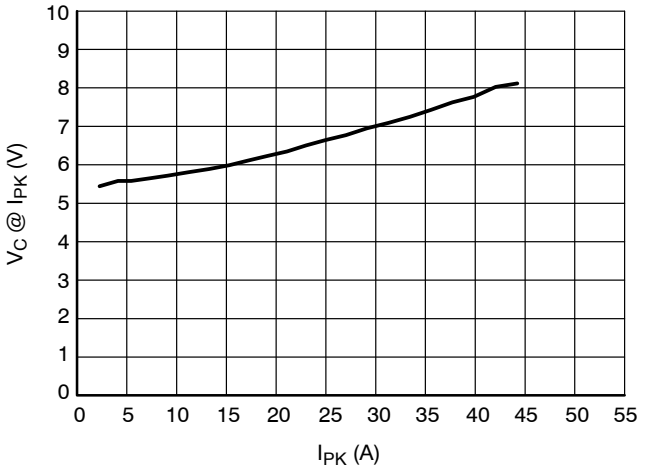


Figure 6. Negative Clamping Voltage vs. Peak Pulse Current (t_p = 8/20 μs)

TYPICAL CHARACTERISTICS

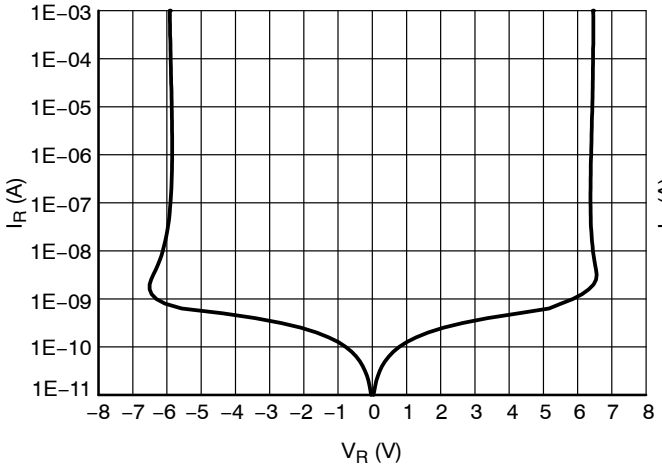


Figure 7. Breakdown Voltage

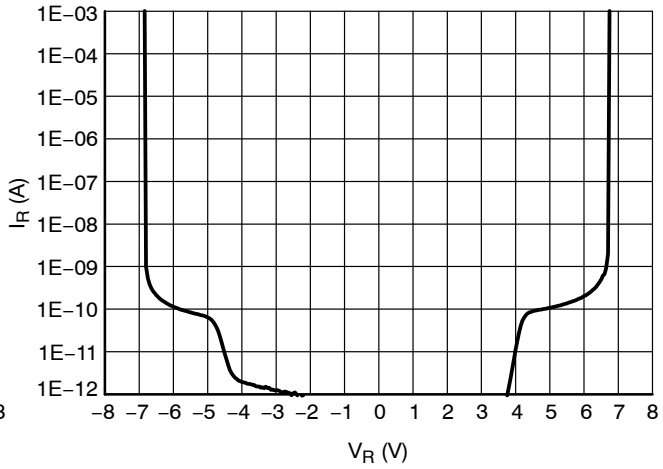


Figure 8. Reverse Leakage Current

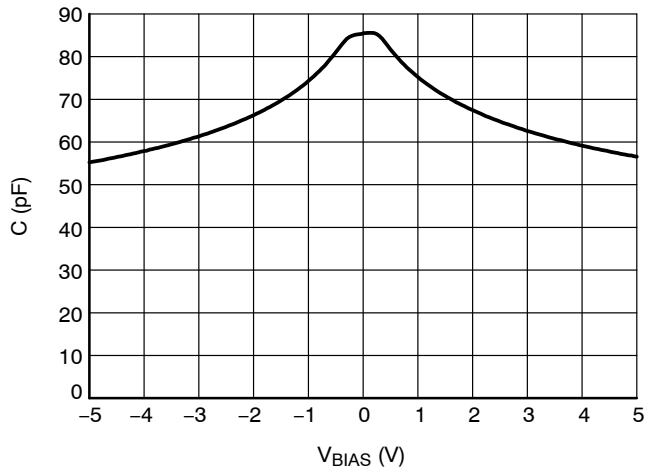


Figure 9. Line Capacitance, *f* = 1 MHz

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 10. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 11 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.

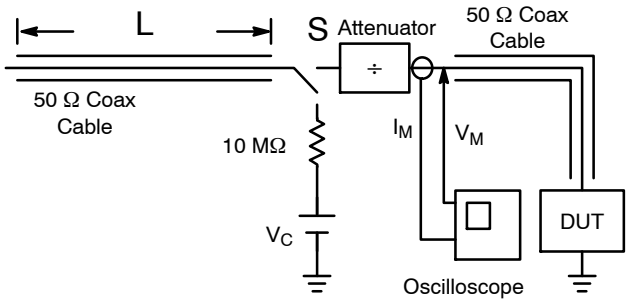


Figure 10. Simplified Schematic of a Typical TLP System

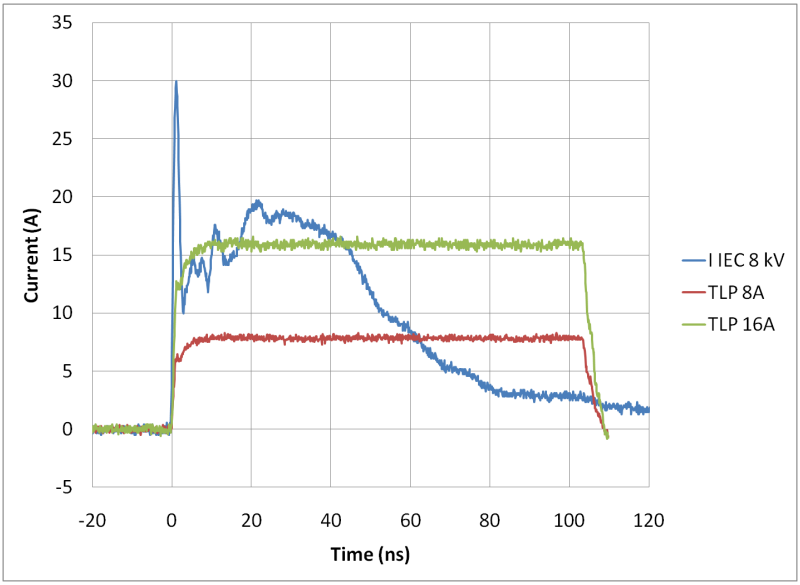


Figure 11. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

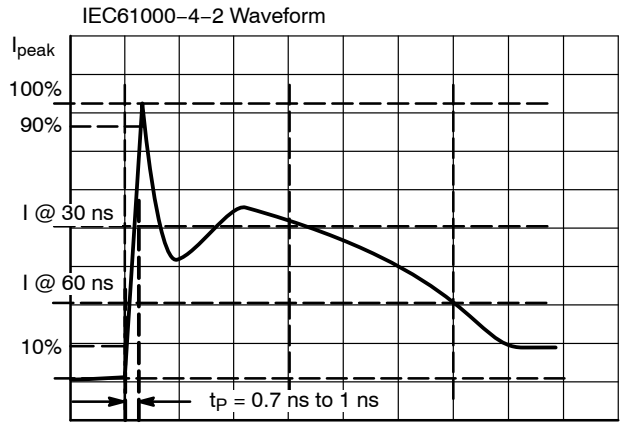


Figure 12. IEC61000−4−2 Spec

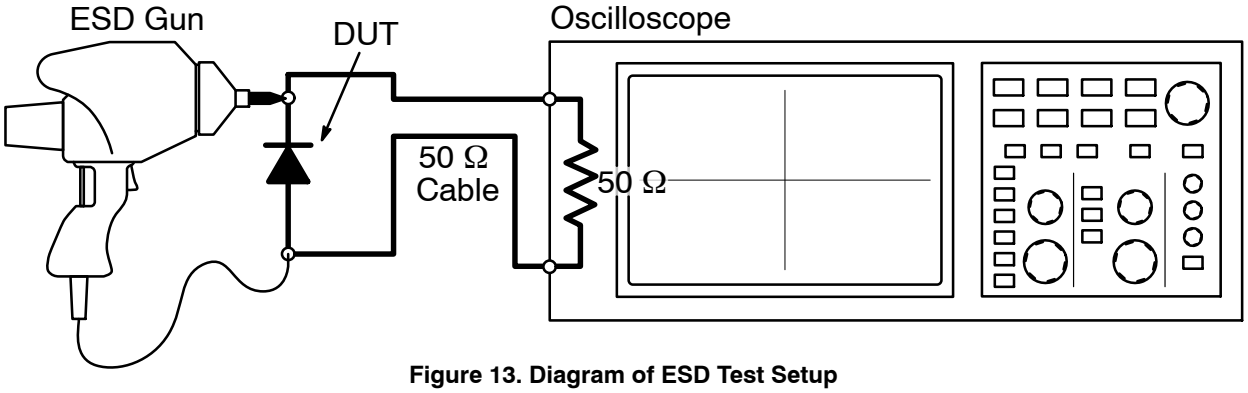


Figure 13. Diagram of ESD Test Setup

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

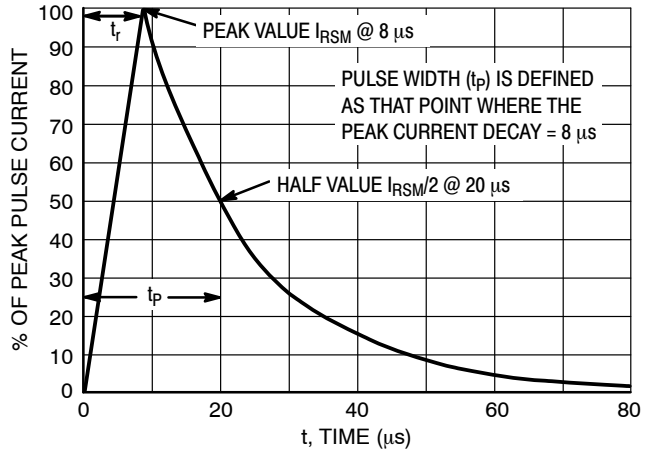
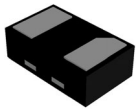
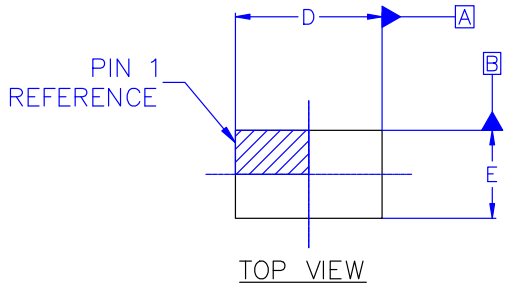


Figure 14. 8 X 20 μs Pulse Waveform

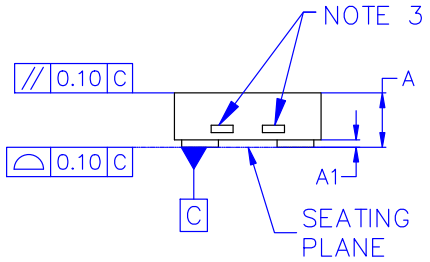


X2DFN−2 1.00x0.60x0.37, 0.65P
CASE 714AB
ISSUE D

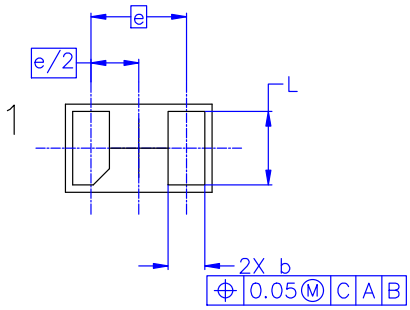
DATE 25 SEP 2026



TOP VIEW



SIDE VIEW

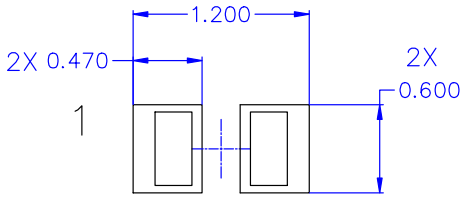


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOW.

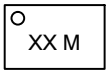
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
A1	−−−	0.03	0.050
b	0.20	0.25	0.30
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	0.65 BSC		
L	0.45	0.50	0.55



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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