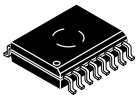
# Isolated High Current IGBT Gate Driver

# NCD57001



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**SOIC−16 WB**
**CASE 751G−03**

NCD57001 is a high−current single channel IGBT driver with internal galvanic isolation, designed for high system efficiency and reliability in high power applications. Its features include complementary inputs, open drain FAULT and Ready outputs, active Miller clamp, accurate UVLOs, DESAT protection, and soft turn−off at DESAT. NCD57001 accommodates both 5 V and 3.3 V signals on the input side and wide bias voltage range on the driver side including negative voltage capability. NCD57001 provides > 5 kVrms (UL1577 rating) galvanic isolation and > 1200 $V_{IORM}$ (working voltage) capabilities. NCD57001 is available in the wide−body SOIC−16 package with guaranteed 8 mm creepage distance between input and output to fulfill reinforced safety insulation requirements.

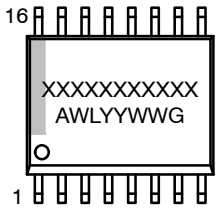
### Features

- High Current Output (+4/−6 A) at IGBT Miller Plateau Voltages
- Low Output Impedance for Enhanced IGBT Driving
- Short Propagation Delays with Accurate Matching
- Active Miller Clamp to Prevent Spurious Gate Turn−on
- DESAT Protection with Programmable Delay
- Negative Voltage (Down to −9 V) Capability for DESAT
- Soft Turn Off During IGBT Short Circuit
- IGBT Gate Clamping During Short Circuit
- IGBT Gate Active Pull Down
- Tight UVLO Thresholds for Bias Flexibility
- Wide Bias Voltage Range including Negative VEE2
- 3.3 V to 5 V Input Supply Voltage
- Designed for AEC−Q100 Certification
- 5000 V Galvanic Isolation (to meet UL1577 Requirements)
- 1200 V Working Voltage (per VDE0884−10 Requirements)
- High Transient Immunity
- High Electromagnetic Immunity
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

### Typical Applications

- Solar Inverters
- Motor Control
- Uninterruptible Power Supplies (UPS)
- Industrial Power Supplies
- Welding

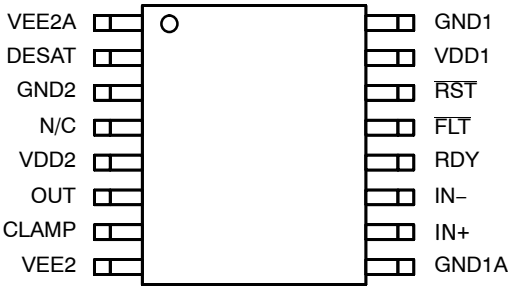
### MARKING DIAGRAM




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

### PIN ASSIGNMENT




### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

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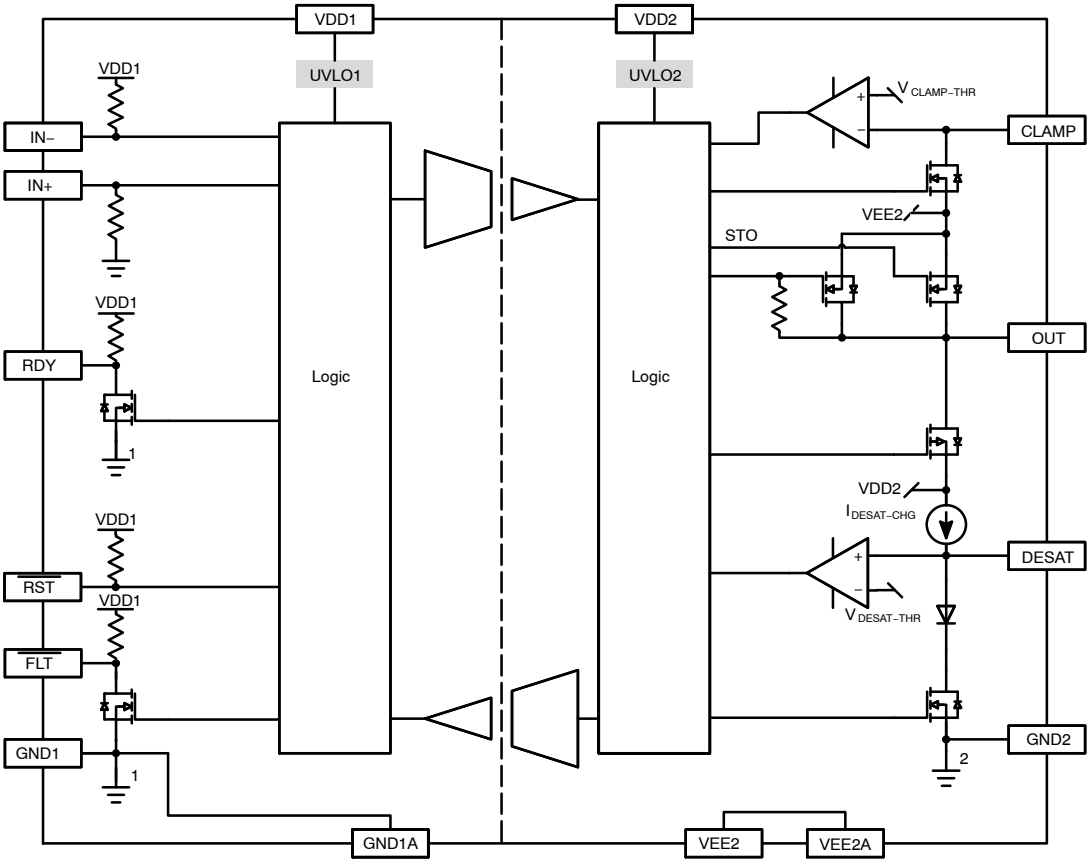


**Figure 1. Simplified Block Diagram**

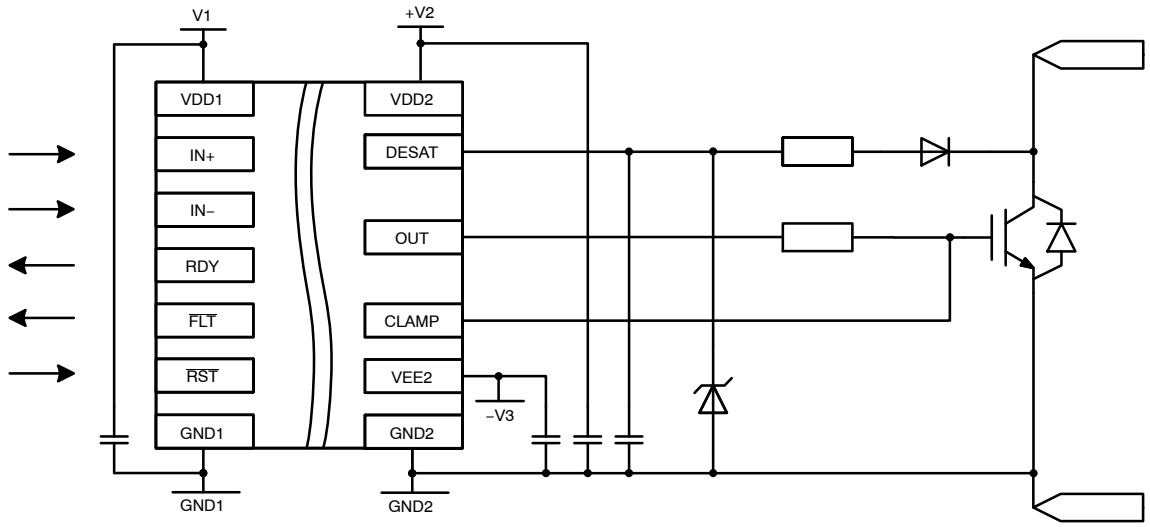


**Figure 2. Simplified Application Schematics**

**PIN DESCRIPTION**

| Pin Name | No. | I/O | Description |
|---|---|---|---|
| $V_{EE2A}$ | 1 | Power | Output side negative power supply. A good quality bypassing capacitor is required from these pins to GND2 and should be placed close to the pins for best results. Connect it to GND2 for unipolar supply application. |
| $V_{EE2}$ | 8 | | |
| DESAT | 2 | I/O | Input for detecting the desaturation of IGBT due to a short circuit condition. An internal constant current source $I_{DESAT-CHG}$ charging an external capacitor connected to this pin allows a programmable blanking delay every ON cycle before DESAT fault is processed, thus preventing false triggering. When the DESAT voltage goes up and reaches $V_{DESAT-THR}$, the output is driven low. Further, the /FLT output is activated, please refer to Figure 5 on page 10.<br><br>A 5 μs mute time apply to IN+ and IN− once DESAT occurs. |
| GND2 | 3 | Power | Output side gate drive reference connecting to IGBT emitter or FET source. |
| N/C | 4 | – | Not connected. |
| $V_{DD2}$ | 5 | Power | Output side positive power supply. The operating range for this pin is from UVLO2 to its maximum allowed value. A good quality bypassing capacitor is required from this pin to GND2 and should be placed close to the pins for best results. |
| OUT | 6 | O | Driver output that provides the appropriate drive voltage and source/sink current to the IGBT/FET gate. OUT is actively pulled low during start−up and under Fault conditions. |
| CLAMP | 7 | I/O | Provides clamping for the IGBT/FET gate during the off period to protect it from parasitic turn−on. Its internal N FET is turned on when the voltage of this pin falls below $V_{EE2}$ + $V_{CLAMP-THR}$. It is to be tied directly to IGBT/FET gate with minimum trace length for best results. |
| GND1 | 9 | Power | Input side ground reference. |
| | 16 | | |
| IN+ | 10 | I | Non inverted gate driver input. It is internally clamped to $V_{DD1}$ and has a pull−down resistor of 50 kΩ to ensure that output is low in the absence of an input signal. A minimum positive going pulse−width is required at IN+ before OUT responds. |
| IN− | 11 | I | Inverted gate driver input. It is internally clamped to $V_{DD1}$ and has a pull−up resistor of 50 kΩ to ensure that output is low in the absence of an input signal. A minimum negative going pulse−width is required at IN− before OUT responds. |
| RDY | 12 | O | Power good indication output, active high when $V_{DD2}$ is good. There is an internal 50 kΩ pull−up resistor connected to this pin. Multiple of them from different drivers can be ”OR”ed together. If a low RDY event is triggered by UVLO2, the maximum low duration for RDY is 200 ns. OUT remains low when RDY is low. Short time delay may apply. See Figure 4 on page 9 for details. |
| /FLT | 13 | O | Fault output (active low) that allows communication to the main controller that the driver has encountered a desaturation condition and has deactivated the output. |
| /RST | 14 | I | Reset input with an internal 50 kΩ pull−up resistor, active low to reset fault latch. |
| $V_{DD1}$ | 15 | Power | Input side power supply (3.3 V to 5 V). |

## SAFETY AND INSULATION RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| | Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage | < 150 $V_{RMS}$ | I – IV | |
| | | < 300 $V_{RMS}$ | I – IV | |
| | | < 450 $V_{RMS}$ | I – IV | |
| | | < 600 $V_{RMS}$ | I – IV | |
| | | < 1000 $V_{RMS}$ | I – III | |
| CTI | Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1) | | 600 | |
| | Climatic Classification | | 40/100/21 | |
| | Polution Degree (DIN VDE 0110/1.89) | | 2 | |
| $V_{PR}$ | Input−to−Output Test Voltage, Method b, $V_{IORM}$ x 1.875 = $V_{PR}$, 100% Production Test with tm = 1 s, Partial Discharge < 5 pC | | 2250 | $V_{pk}$ |
| | Input−to−Output Test Voltage, Method a, $V_{IORM}$ x 1.6 = $V_{PR}$, Type and Sample Test with tm = 10 s, Partial Discharge < 5 pC | | – | $V_{pk}$ |
| $V_{IORM}$ | Maximum Repetitive Peak Voltage | | 1200 | $V_{pk}$ |
| $V_{IOWM}$ | Maximum Working Insulation Voltage | | 870 | $V_{RMS}$ |
| $V_{IOTM}$ | Highest Allowable Over Voltage | | 8400 | $V_{pk}$ |
| $E_{CR}$ | External Creepage | | 8.0 | mm |
| $E_{CL}$ | External Clearance | | 8.0 | mm |
| DTI | Insulation Thickness | | 17.3 | um |
| $T_{Case}$ | Safety Limit Values – Maximum Values in Failure; Case Temperature | | 150 | °C |
| $P_{S,INPUT}$ | Safety Limit Values – Maximum Values in Failure; Input Power | | 36 | mW |
| $P_{S,OUTPUT}$ | Safety Limit Values – Maximum Values in Failure; Output Power | | 1364 | mW |
| $R_{IO}$ | Insulation Resistance at TS, $V_{IO}$ = 500 V | | $10^9$ | Ω |

**ABSOLUTE MAXIMUM RATINGS** (Over operating free−air temperature range unless otherwise noted) (Note 1)

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{DD1}$−GND1 | Supply voltage, input side | −0.3 | 6 | V |
| $V_{DD2}$−GND2 | Positive Power Supply, output side | −0.3 | 25 | V |
| $V_{EE2}$−GND2 | Negative Power Supply, output side | −10 | 0.3 | V |
| $V_{DD2}$−$V_{EE2}$ ($V_{MAX2}$) | Differential Power Supply, output side | 0 | 25 | V |
| $V_{OUT}$ | Gate−driver output voltage | $V_{EE2}$ − 0.3 | $V_{DD2}$ + 0.3 | V |
| $I_{PK-SRC}$ | Gate−driver output sourcing current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, $V_{MAX2}$ = 20 V) | − | 7.8 | A |
| $I_{PK-SNK}$ | Gate−driver output sinking current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, $V_{MAX2}$ = 20 V) | − | 7.1 | A |
| $I_{PK-CLAMP}$ | Clamp sinking current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, $V_{CLAMP}$ = 3 V) | − | 2.5 | A |
| $t_{CLP}$ | Maximum Short Circuit Clamping Time ($I_{OUT_CLAMP}$ = 500 mA) | − | 10 | μs |
| $V_{LIM}$−GND1 | Voltage at IN+, IN−, /RST, /FLT, RDY | −0.3 | $V_{DD1}$ + 0.3 | V |
| $I_{LIM}$−GND1 | Output current of /FLT, RDY | − | 10 | mA |
| $V_{DESAT}$−GND2 | Desat Voltage (Note 2) | −9 | $V_{DD2}$ + 0.3 | V |
| $V_{CLAMP}$−GND2 | Clamp Voltage | $V_{EE2}$ − 0.3 | $V_{DD2}$ + 0.3 | V |
| $P_D$ | Power Dissipation (Note 3) | − | 1400 | mW |
| $T_{J(max)}$ | Maximum Junction Temperature | −40 | 150 | °C |
| $T_{STG}$ | Storage Temperature Range | −65 | 150 | °C |
| $ESD_{HBM}$ | ESD Capability, Human Body Model (Note 4) | − | ±2 | kV |
| $ESD_{CDM}$ | ESD Capability, Charged Device Model (Note 4) | − | ±2 | kV |
| MSL | Moisture Sensitivity Level | − | 2 | − |
| $T_{SLD}$ | Lead Temperature Soldering Reflow, Pb−Free Versions (Note 5) | − | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. The minimum value is verified by characterization with a single pulse of 100 mA for 100 μs.
3. The value is estimated for ambient temperature 25°C and junction temperature 150°C, 650 $mm^2$, 1 oz copper, 2 surface layers and 2 internal power plane layers. Power dissipation is affected by the PCB design and ambient temperature.
4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101)
   Latchup Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78, 25°C
5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**THERMAL CHARACTERISTICS**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Air | 100 $mm^2$, 1 oz Copper, 1 Surface Layer | 114 | °C/W |
| | | 650 $mm^2$, 1 oz Copper, 2 Surface Layers and 2 Internal Power Plane Layers | 62 | |

**OPERATING RANGES** (Note 6)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD1}$–GND1 | Supply voltage, input side | UVLO1 | 5.5 | V |
| $V_{DD2}$–GND2 | Positive Power Supply, output side | UVLO2 | 24 | V |
| $V_{EE2}$–GND2 | Negative Power Supply, output side | –10 | 0 | V |
| $V_{DD2}$–$V_{EE2}$ ($V_{MAX2}$) | Differential Power Supply, output side | 0 | 24 | V |
| $V_{IL}$ | Low level input voltage at IN+, IN–, /RST | 0 | 0.3 X $V_{DD1}$ | V |
| $V_{IH}$ | High level input voltage at IN+, IN–, /RST | 0.7 X $V_{DD1}$ | $V_{DD1}$ | V |
| $\|dV_{ISO}/dt\|$ | Common Mode Transient Immunity (1500 V) | 100 | – | kV/μs |
| $T_A$ | Ambient Temperature | –40 | 125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

**ISOLATION CHARACTERISTICS**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ISO,\ input-output}$ | Input–Output Isolation Voltage | $T_A$ = 25°C, Relative Humidity < 50%, t = 1.0 minute, $I_{I-O}$ 10 A, 50 Hz (See Note 7, 8, 9) | 5000 | – | – | $V_{RMS}$ |
| $R_{ISO}$ | Isolation Resistance | $V_{I-O}$ = 500 V (See Note 7) | – | $10^{11}$ | – | Ω |

7. Device is considered a two–terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together
8. 5,000 $V_{RMS}$ for 1–minute duration is equivalent to 6,000 $V_{RMS}$ for 1–second duration.
9. The input–output isolation voltage is a dielectric voltage rating per UL1577. It should not be regarded as an input–output continuous voltage rating. For the continuous working voltage rating, refer to equipment–level safety specification or DIN VDE V 0884–11 Safety and Insulation Ratings Table

**ELECTRICAL CHARACTERISTICS** ($V_{DD1}$ = 5 V, $V_{DD2}$ = 15 V, $V_{EE2}$ = –8 V. For typical values $T_A$ = 25°C, for min/max values, $T_A$ is the operating ambient temperature range that applies, unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VOLTAGE SUPPLY** | | | | | | |
| $V_{UVLO1-OUT-ON}$ | UVLO1 Output Enabled | | – | – | 3 | V |
| $V_{UVLO1-OUT-OFF}$ | UVLO1 Output Disabled | | 2.4 | – | – | V |
| $V_{UVLO1-HYST}$ | UVLO1 Hysteresis | | 0.125 | – | – | V |
| $V_{UVLO2-OUT-ON}$ | UVLO2 Output Enabled | | 13.2 | 13.5 | 13.8 | V |
| $V_{UVLO2-OUT-OFF}$ | UVLO2 Output Disabled | | 12.2 | 12.5 | 12.8 | V |
| $V_{UVLO2-HYST}$ | UVLO2 Hysteresis | | – | 1 | | V |
| $I_{DD1-0}$ | Input Supply Quiescent Current Output Low | IN+ = Low, IN– = Low<br>RDY = High, /FLT = High | – | 1 | 2 | mA |
| $I_{DD1-100}$ | Input Supply Quiescent Current Output High | IN+ = High, IN– = Low<br>RDY = High, /FLT = High | – | 4.8 | 6 | mA |
| $I_{DD2-0}$ | Output Positive Supply Quiescent Current, Output Low | IN+ = Low, IN– = Low<br>RDY = High, /FLT = High, no load | – | 3.3 | 4 | mA |
| $I_{DD2-100}$ | Output Positive Supply Quiescent Current, Output High | IN+ = High, IN– = Low<br>RDY = High, /FLT = High, no load | – | 3.6 | 6 | mA |
| $I_{EE2-0}$ | Output Negative Supply Quiescent Current, Output Low | IN+ = High, IN– = Low, no load | – | 0.4 | 2 | mA |
| $I_{EE2-100}$ | Output Negative Supply Quiescent Current, Output High | IN+ = High, IN– = Low, no load | – | 0.2 | 2 | mA |

**ELECTRICAL CHARACTERISTICS** ($V_{DD1}$ = 5 V, $V_{DD2}$ = 15 V, $V_{EE2}$ = −8 V. For typical values $T_A$ = 25°C, for min/max values, $T_A$ is the operating ambient temperature range that applies, unless otherwise noted) (continued)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LOGIC INPUT AND OUTPUT** | | | | | | |
| $V_{IL}$ | IN+, IN−, /RST Low Input Voltage | | − | − | 0.3 x $V_{DD1}$ | V |
| $V_{IH}$ | IN+, IN−, /RST High Input Voltage | | 0.7 x $V_{DD1}$ | − | − | V |
| $V_{IN-HYST}$ | Input Hysteresis Voltage | | − | 0.15 x $V_{DD1}$ | − | V |
| $I_{IN-L}$, $I_{RST-L}$ | IN−, /RST Input Current (50 kΩ pull−up resistor) | $V_{IN-}$/$V_{RST}$ = 0 V | − | −100 | − | μA |
| $I_{IN+H}$ | IN+ Input Current (50 kΩ pull−down resistor) | $V_{IN+}$ = 5 V | − | 100 | − | μA |
| $I_{RDY-L}$, $I_{FLT-L}$ | RDY, /FLT Pull−up Current (50 kΩ pull−up resistor) | $V_{RDY}$/$V_{FLT}$ = Low | − | 100 | − | μA |
| $V_{RDY-L}$, $V_{FLT-L}$ | RDY, /FLT Low Level Output Voltage | $I_{RDY}$/$I_{FLT}$ = 5 mA | − | − | 0.3 | V |
| $t_{MIN1}$ | Input Pulse Width of IN+, IN− for No Response at Output | | − | − | 10 | ns |
| $t_{MIN2}$ | Input Pulse Width of IN+, IN− for Guaranteed Response at Output | | 40 | − | − | ns |
| $t_{RST-MIN}$ | Pulse Width of /RST for Resetting /FLT | | 800 | − | − | ns |
| **DRIVER OUTPUT** | | | | | | |
| $V_{OUTL1}$ | Output Low State ($V_{OUT}$ − $V_{EE2}$) | $I_{SINK}$ = 200 mA | − | 0.1 | 0.2 | V |
| $V_{OUTL3}$ | | $I_{SINK}$ = 1.0 A, $T_A$ = 25°C | − | 0.5 | 0.8 | |
| $V_{OUTH1}$ | Output High State ($V_{DD2}$ − $V_{OUT}$) | $I_{SRC}$ = 200 mA | − | 0.3 | 0.5 | V |
| $V_{OUTH3}$ | | $I_{SRC}$ = 1.0 A, $T_A$ = 25°C | − | 0.8 | 1 | |
| $I_{PK-SNK1}$ | Peak Driver Current, Sink (Note 10) | $V_{OUT}$ = 7.9 V | − | 7.1 | − | A |
| $I_{PK-SRC1}$ | Peak Driver Current, Source (Note 10) | $V_{OUT}$ = −5 V | − | 7.8 | − | A |
| **MILLER CLAMP** | | | | | | |
| $V_{CLAMP}$ | Clamp Voltage ($V_{CLAMP}$ − $V_{EE2}$) | $I_{CLAMP}$ = 2.5 A, $T_A$ = 25°C | − | 1.3 | 1.7 | V |
| | | $I_{CLAMP}$ = 2.5 A, $T_A$ = −40°C to 125°C | − | − | 3 | |
| $V_{CLAMP-THR}$ | Clamp Activation Threshold ($V_{CLAMP}$ − $V_{EE2}$) | | 1.5 | 2 | 2.5 | V |
| **IGBT SHORT CIRCUIT CLAMPING** | | | | | | |
| $V_{CLAMP-OUT}$ | Clamping Voltage, ($V_{OUT}$ − $V_{DD2}$) | IN+ = Low, IN− = High, $I_{OUT}$ = 500 mA (pulse test, $t_{CLPmax}$ = 10 μs) | − | 0.9 | 1.1 | V |
| $V_{CLAMP-CLAMP}$ | Clamping Voltage, Clamp ($V_{CLAMP}$ − $V_{DD2}$) | IN+ = High, IN− = Low, $I_{CLAMP-CLAMP}$ = 500 mA (pulse test, $t_{CLPmax}$ = 10 μs) | − | 1.4 | 1.6 | V |
| **DESAT PROTECTION** | | | | | | |
| $V_{DESAT-THR}$ | DESAT Threshold Voltage | | 8.5 | 9 | 9.5 | V |
| $V_{DESAT-NEG}$ | DESAT Negative Voltage | $I_{DESAT}$ = 1.5 mA | − | −8 | − | V |
| $I_{DESAT-CHG}$ | Blanking Charge Current | $V_{DESAT}$ = 7 V | 0.45 | 0.5 | 0.6 | mA |
| $I_{DESAT-DIS}$ | Blanking Discharge Current | | − | 50 | − | mA |

**ELECTRICAL CHARACTERISTICS** ($V_{DD1}$ = 5 V, $V_{DD2}$ = 15 V, $V_{EE2}$ = −8 V. For typical values $T_A$ = 25°C, for min/max values, $T_A$ is the operating ambient temperature range that applies, unless otherwise noted) (continued)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $t_{PD-ON}$ | IN+, IN− to Output High Propagation Delay | $C_{LOAD}$ = 10 nF<br>$V_{IH}$ to 10% of output change for PW > 150 ns. OUT and CLAMP pins are connected together | 40 | 60 | 90 | ns |
| $t_{PD-OFF}$ | IN+, IN− to Output Low Propagation Delay | $C_{LOAD}$ = 10 nF<br>$V_{IL}$ to 90% of output change for PW > 150 ns. OUT and CLAMP pins are connected together | 40 | 66 | 90 | ns |
| $t_{DISTORT}$ | Propagation Delay Distortion (= $t_{PD-ON} - t_{PD-OFF}$) | $T_A$ = 25°C, PW > 150 ns | −15 | −6 | 15 | ns |
| | | $T_A$ = −40°C to 125°C, PW > 150 ns | −25 | – | 25 | |
| $t_{DISTORT_TOT}$ | Prop Delay Distortion between Parts | PW > 150 ns | −30 | 0 | 30 | ns |
| $t_{RISE}$ | Rise Time (see Fig. 3) (Note 10) | $C_{LOAD}$ = 1 nF, 10% to 90% of Output Change | – | 10 | – | ns |
| $t_{FALL}$ | Fall Time (see Fig. 3) (Note 10) | $C_{LOAD}$ = 1 nF, 90% to 10% of Output Change | – | 15 | – | ns |
| $t_{LEB}$ | DESAT Leading Edge Blanking Time (See Fig. 5) | | – | 450 | – | ns |
| $t_{FILTER}$ | DESAT Threshold Filtering Time (see Fig. 5) | | – | 320 | – | ns |
| $t_{STO}$ | Soft Turn Off Time (see Fig. 5) | $C_{LOAD}$ = 10 nF, $R_G$ = 10 Ω. $V_{EE2}$ = 0 V | – | 1.8 | – | μs |
| | | $C_{LOAD}$ = 10 nF, $R_G$ = 10 Ω | – | 2.6 | – | |
| $t_{FLT}$ | Delay after $t_{FILTER}$ to /FLT | | – | 450 | – | ns |
| $t_{RST}$ | /RST Rise to /FLT Rise Delay | | – | 23 | – | ns |
| $t_{RDY1O}$ | RDY High to Output High Delays (see Fig. 4) | | – | 55 | – | ns |
| $t_{RDY2O}$ | | | | | | |
| $t_{RDY1F}$ | $V_{UVLO2-OUT-OFF}$ to RDY Low Delays (see Fig. 4) | | – | 8 | – | μs |
| $t_{RDY2F}$ | | | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

10. Values based on design and/or characterization.

## ORDERING INFORMATION

| Device | Package Type | Shipping† |
|---|---|---|
| NCD57001DWR2G | SOIC−16 Wide Body (Pb−Free) | 1,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

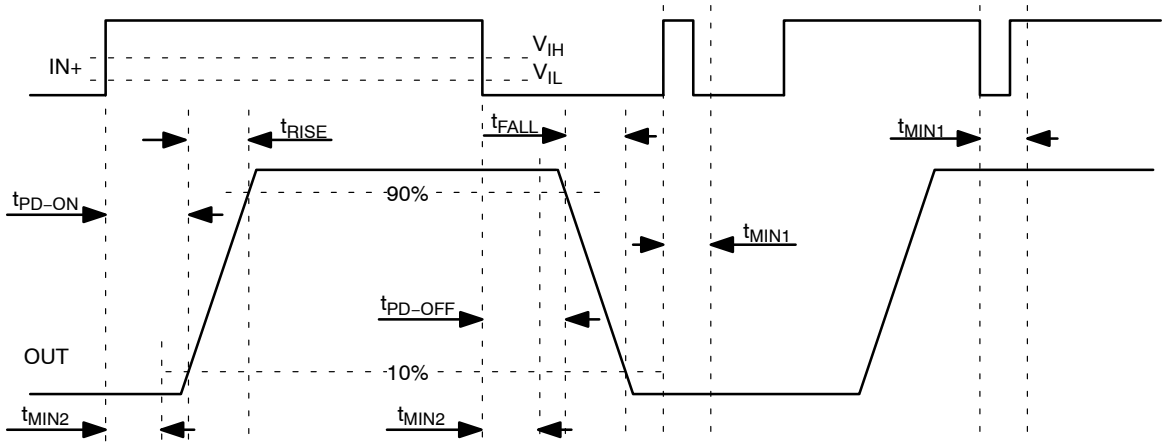


**Figure 3. Propagation Delay, Rise and Fall Time**

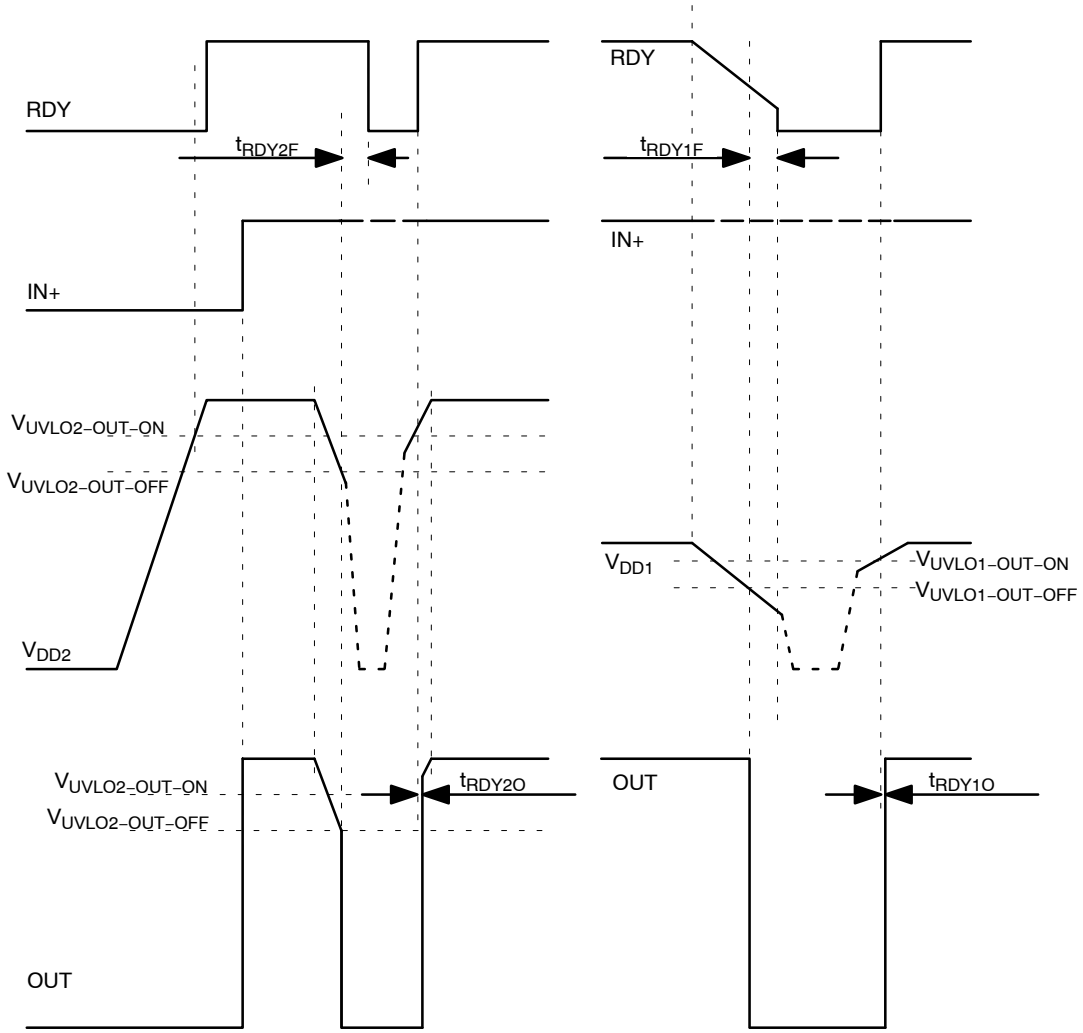


**Figure 4. UVLO Waveform**

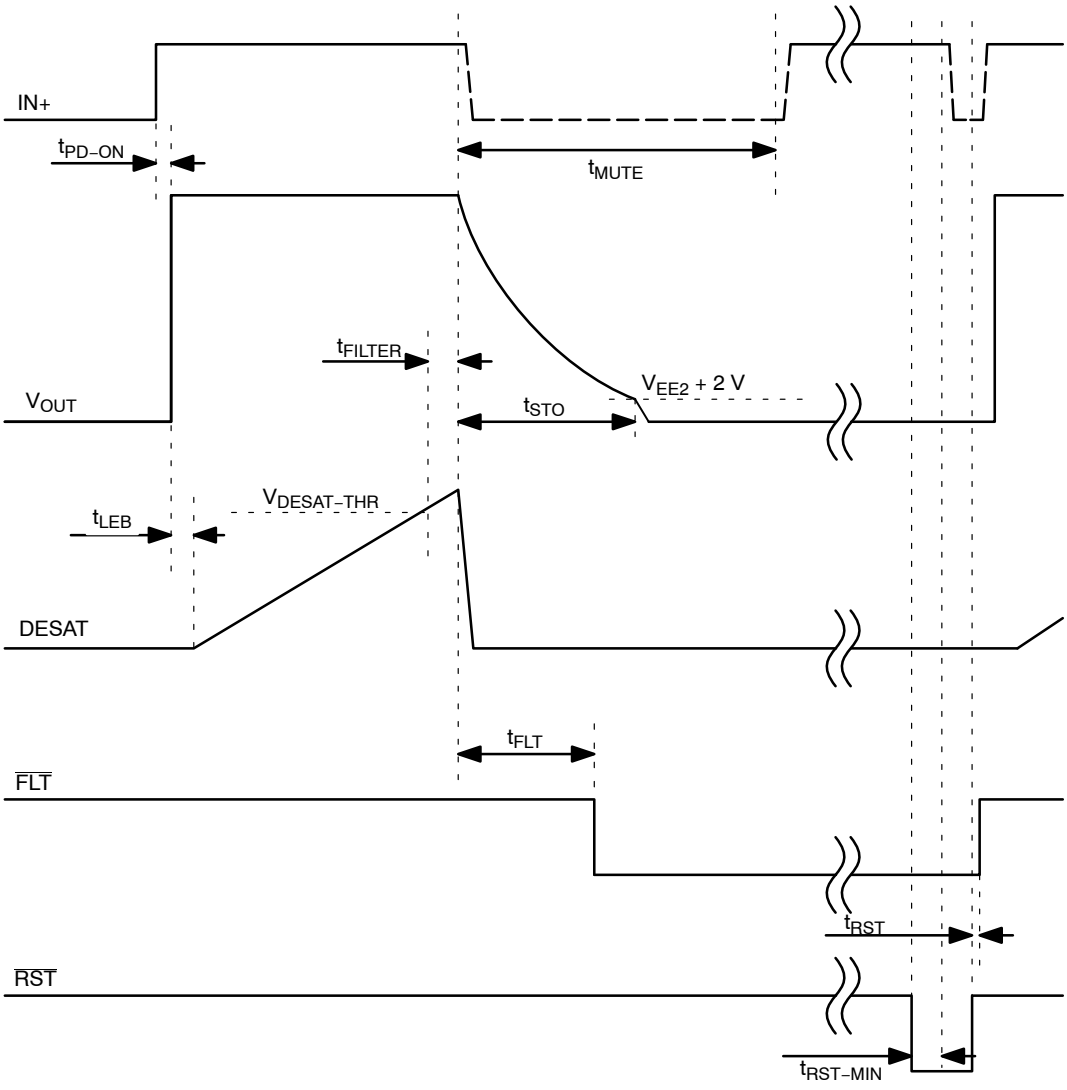


**Figure 5. DESAT Response Waveform**

## TYPICAL CHARACTERISTICS

(Conditions for the following figures are the same as stated for ELECTRICAL CHARACTERISTICS Table unless otherwise noted. Typical and/or average values are used.)

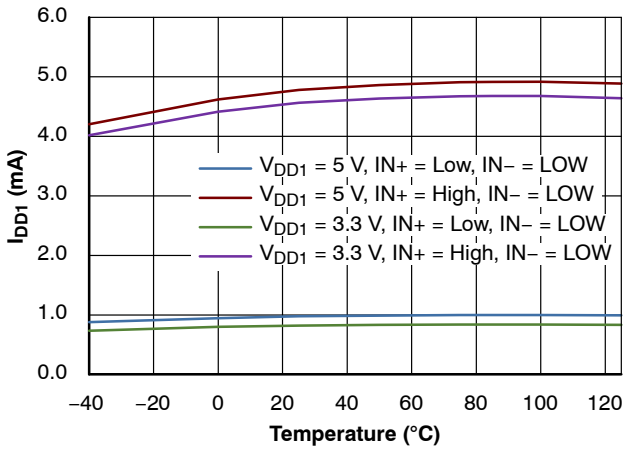


**Figure 6. $V_{DD1}$ Supply Current**

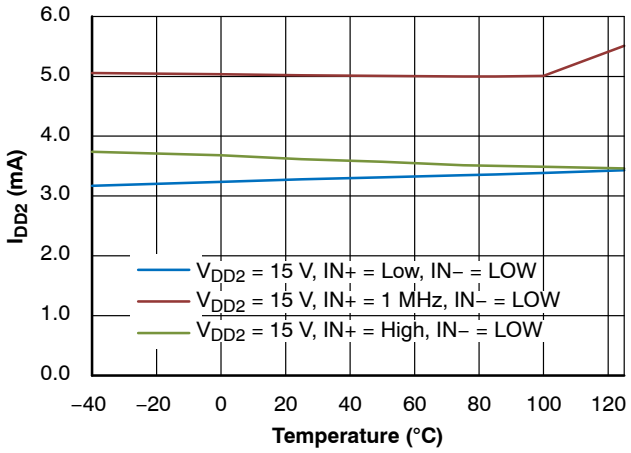


**Figure 7. $V_{DD2}$ Supply Current**

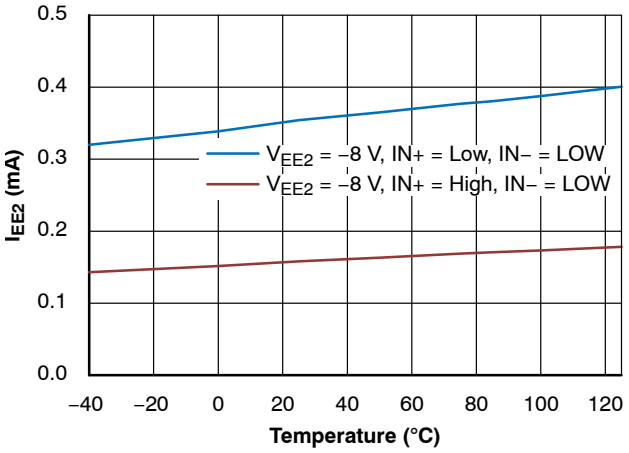


**Figure 8. $V_{EE2}$ Supply Current**

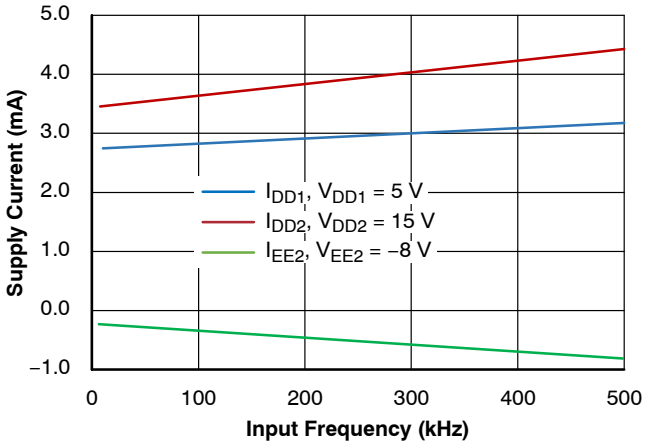


**Figure 9. Supply Current vs Frequency**

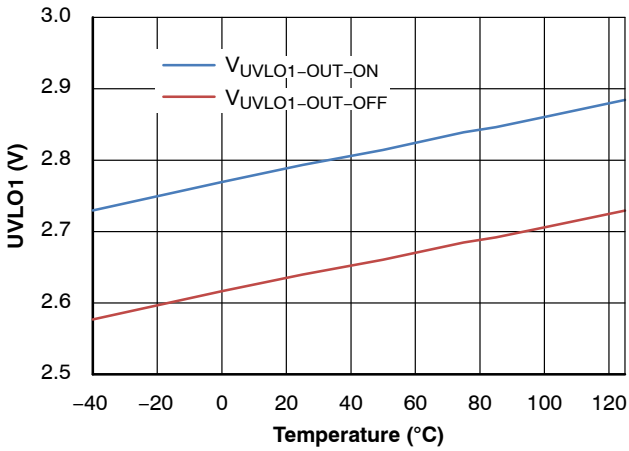


**Figure 10. UVLO1 Threshold Voltage**

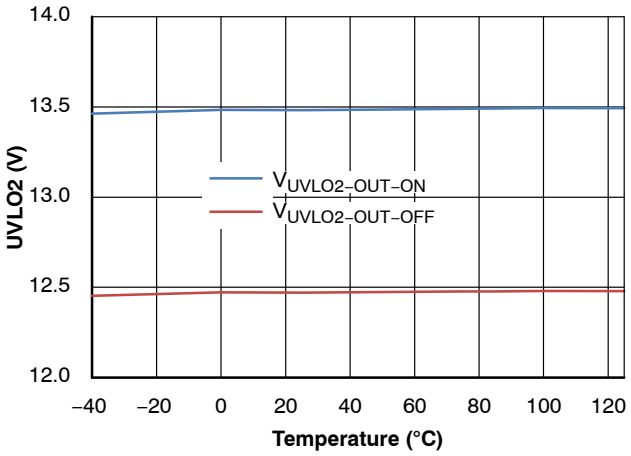


**Figure 11. UVLO2 Threshold Voltage**

## TYPICAL CHARACTERISTICS

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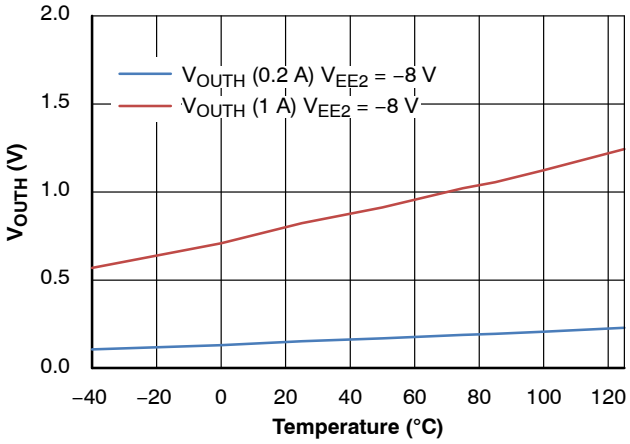



**Figure 12. Output Voltage Drop, Sourcing**

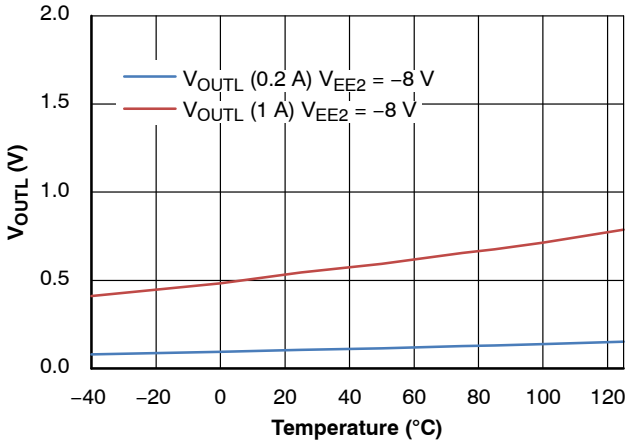



**Figure 13. Output Voltage Drop, Sinking**

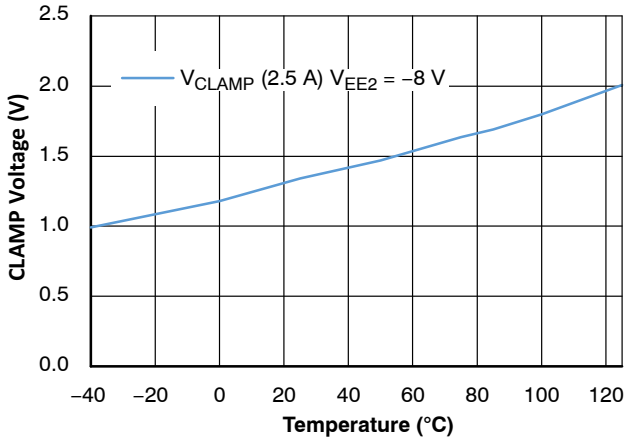



**Figure 14. CLAMP Voltage Drop**

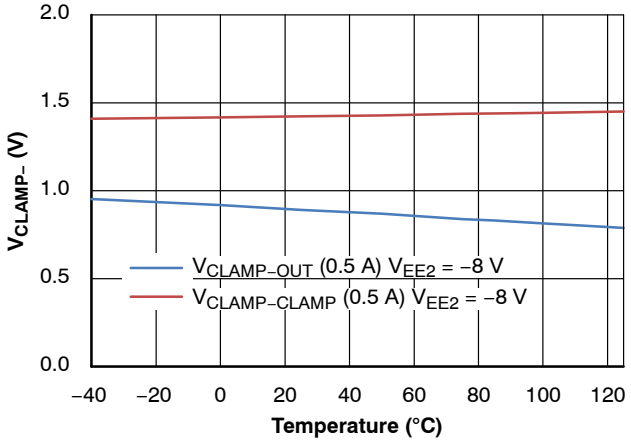



**Figure 15. IGBT Short Circuit Clamp Voltage Drop**

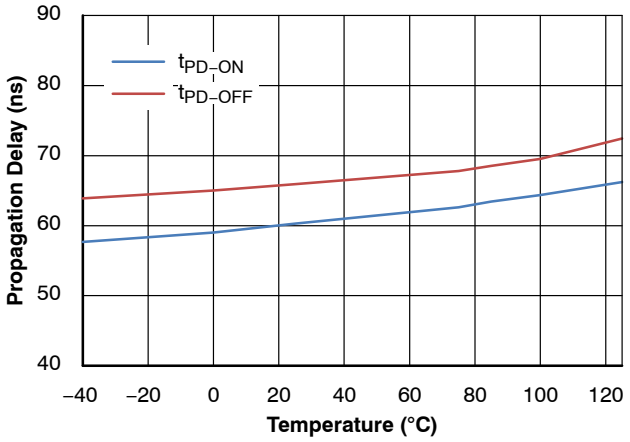



**Figure 16. Propagation Delay**

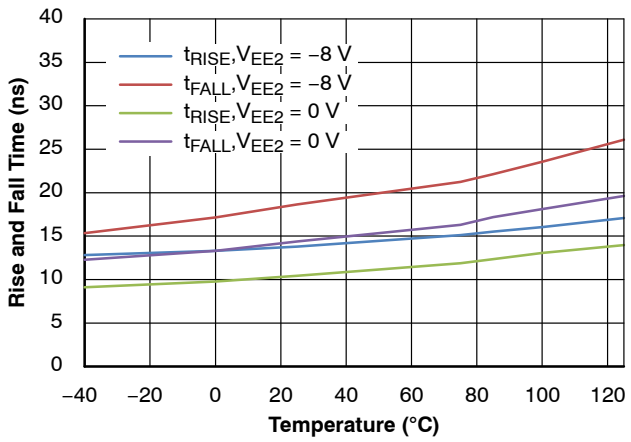



**Figure 17. Rise and Fall Time**

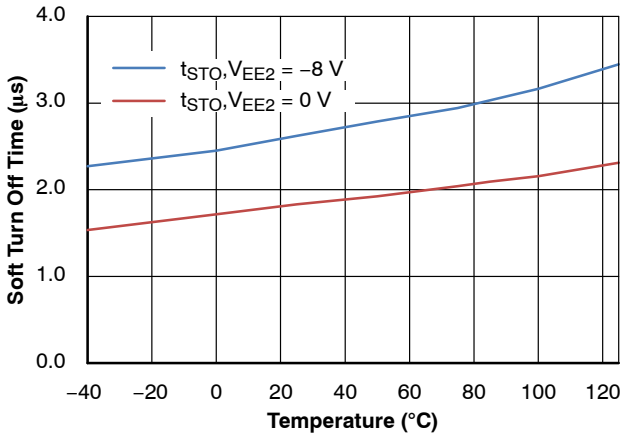



**Figure 18. Soft Turn Off Time**

## FEATURE DESCRIPTIONS

### Under Voltage Lockout (UVLO)

UVLO ensures correct switching of IGBT connected to the driver output.

- The IGBT is turned−off, if the supply $V_{CC1}$ drops below $V_{UVLO1-OUT-OFF}$ and the RDY pin output goes to low.
- The driver output does not start to react to the input signal on $V_{IN}$ until the $V_{CC1}$ rises above the $V_{UVLO1-OUT-ON}$ again. If the supply $V_{CC1}$ increase over $V_{UVLO1-OUT-ON}$, the RDY pin output goes to be open−drain and outputs continue to switch IGBT
- The IGBT is turned−off, if the supply $V_{CC2}$ drops below $V_{UVLO2-OUT-OFF}$ and the RDY pin output goes to low.
- The driver output does not start to react to the input signal on $V_{IN}$ until the $V_{CC1}$ rises above the $V_{UVLO1-OUT-ON}$ again. If the supply $V_{DD1}$ increases over $V_{UVLO1-OUT-ON}$, the RDY pin output goes to be open−drain and outputs continue to switch IGBT
- VEE2 is not monitored.

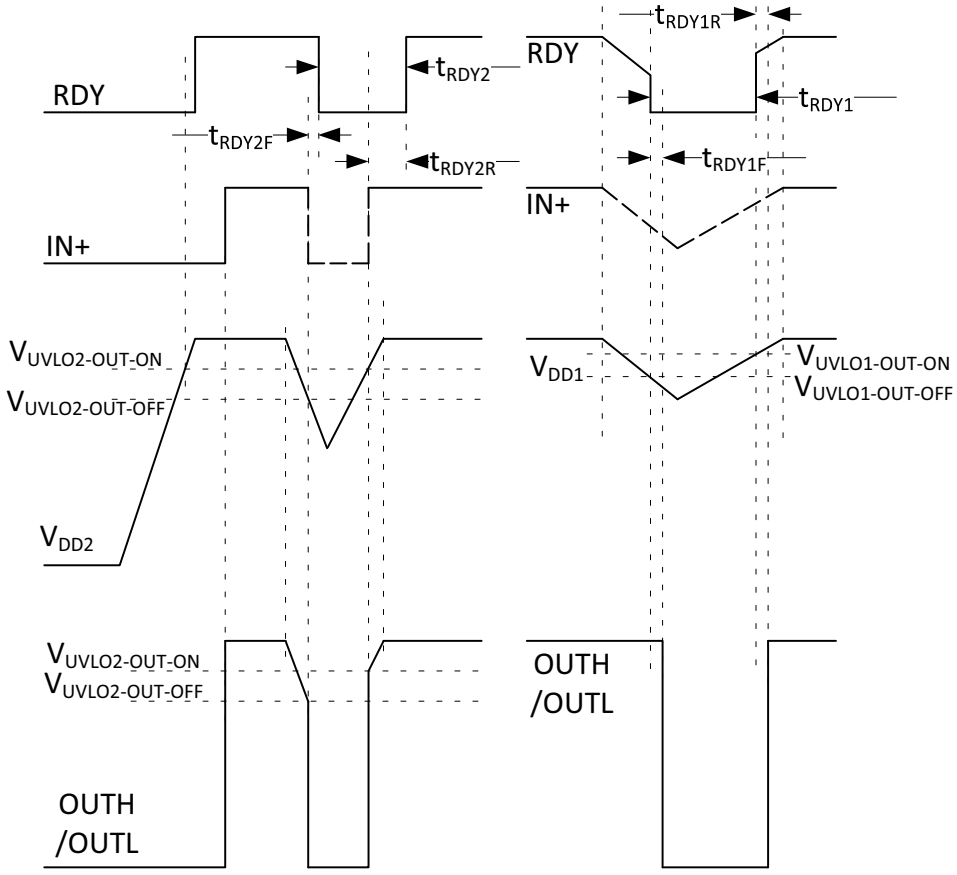



**Figure 19. UVLO Diagram**

### Active Miller Clamp Protection (CLAMP)

NCD57001 supports both bipolar and unipolar power supply with active Miller clamp.

For operation with bipolar supplies, the IGBT is turned off with a negative voltage through OUTL with respect to its emitter. This prevents the IGBT from unintentionally turning on because of current induced from its collector to its gate due to Miller effect. In this condition it is not necessary to connect CLAMP output of the gate driver to the IGBT gate, but connecting CLAMP output to the IGBT gate is also not an issue. Typical values for bipolar operation are $V_{DD2}$ = 15 V and $V_{EE2}$ = −5 V with respect to $GND_2$.

For operation with unipolar supply, typically, $V_{DD2}$ = 15 V with respect to $GND_2$, and $V_{EE2}$ = $GND_2$. In this case, the IGBT can turn on due to additional charge from IGBT Miller capacitance caused by a high voltage slew rate transition on the IGBT collector. To prevent IGBT to turn on, the CLAMP pin is connected directly to IGBT gate and Miller current is sinked through a low impedance CLAMP transistor. When the IGBT is turned−off and the gate voltage transitions below $V_{CLAMP}$, the CLAMP current output is activated.

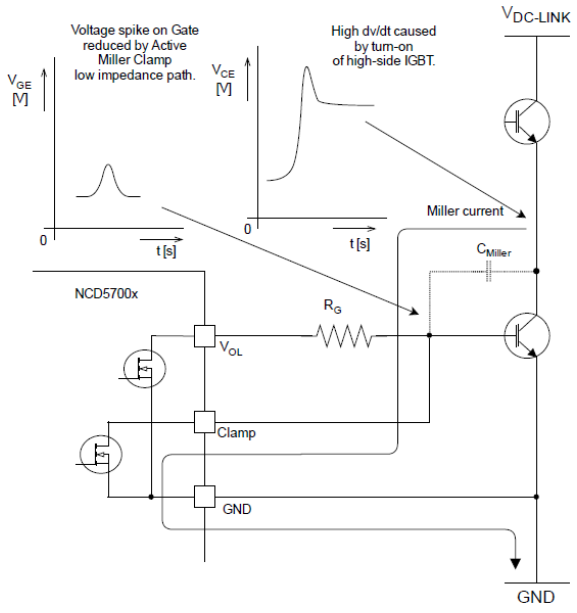



**Figure 20. Current Path without Miler Clamp Protection**

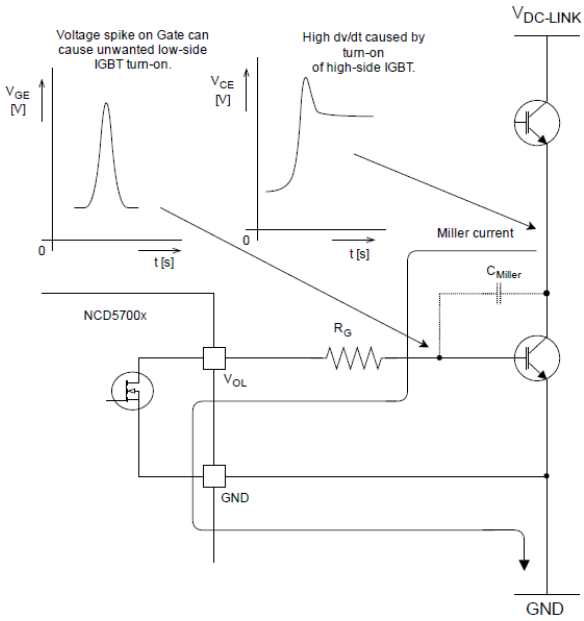



**Figure 21. Current Path with Miler Clamp Protection**

### Non−inverting and Inverting Input Pin (IN+, IN−)

NCD57001 has two possible input modes to control IGBT. Both inputs have defined minimum input pulse width to filter occasional glitches.

- Non−inverting input IN+ controls the driver output while inverting input IN− is set to LOW
- Inverting input IN− controls the driver output while non−inverting input IN+ is set to HIGH

**Warning: When the application use an independent or separate power supply for the control unit ant the input side of the driver, all inputs should be protected by a serial resistor (In case of a power failure of the driver, the driver may be damaged due to overloading of the input protection circuits)**

### Desaturation Protection (DESAT)

Desaturation protection ensures the protection of IGBT at short circuit. When the $V_{CESAT}$ voltage goes up and reaches the set limit, the output is driven low and /FLT output is activated. Blanking time can be set by internal current source and an external capacitor. To avoid false DESAT triggering and minimize blanking time, fast switching diodes with low internal capacitance are recommended. All DESAT protective diodes internal capacitances builds voltage divider with the blanking capacitor.

**Warning: Both external protective diodes are recommended for the protection against voltage spikes caused by IGBT transients passing through parasitic capacitances.**

### DESAT Circuit Parameters Specification

$$t_{BLANK} = C_{BLANK} \cdot \frac{V_{DESAT-THR}}{I_{DESAT-CHG}}$$

$$V_{DESAT-THR} > R_{S-DESAT} \cdot I_{DESAT-CHG} + V_{F\ HV\ diode} + V_{CESAT_IGBT}$$

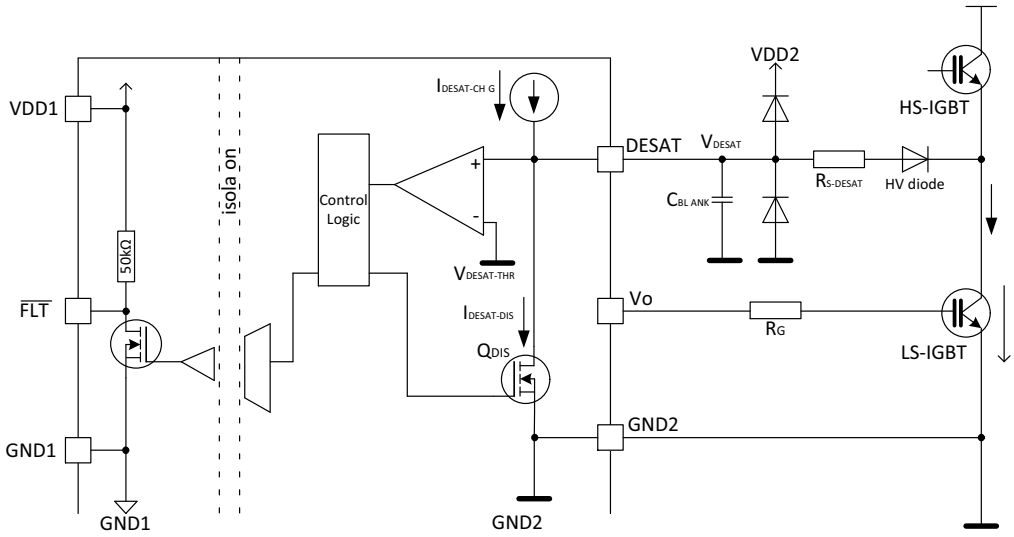



**Figure 22. DESAT Protection Schematic**

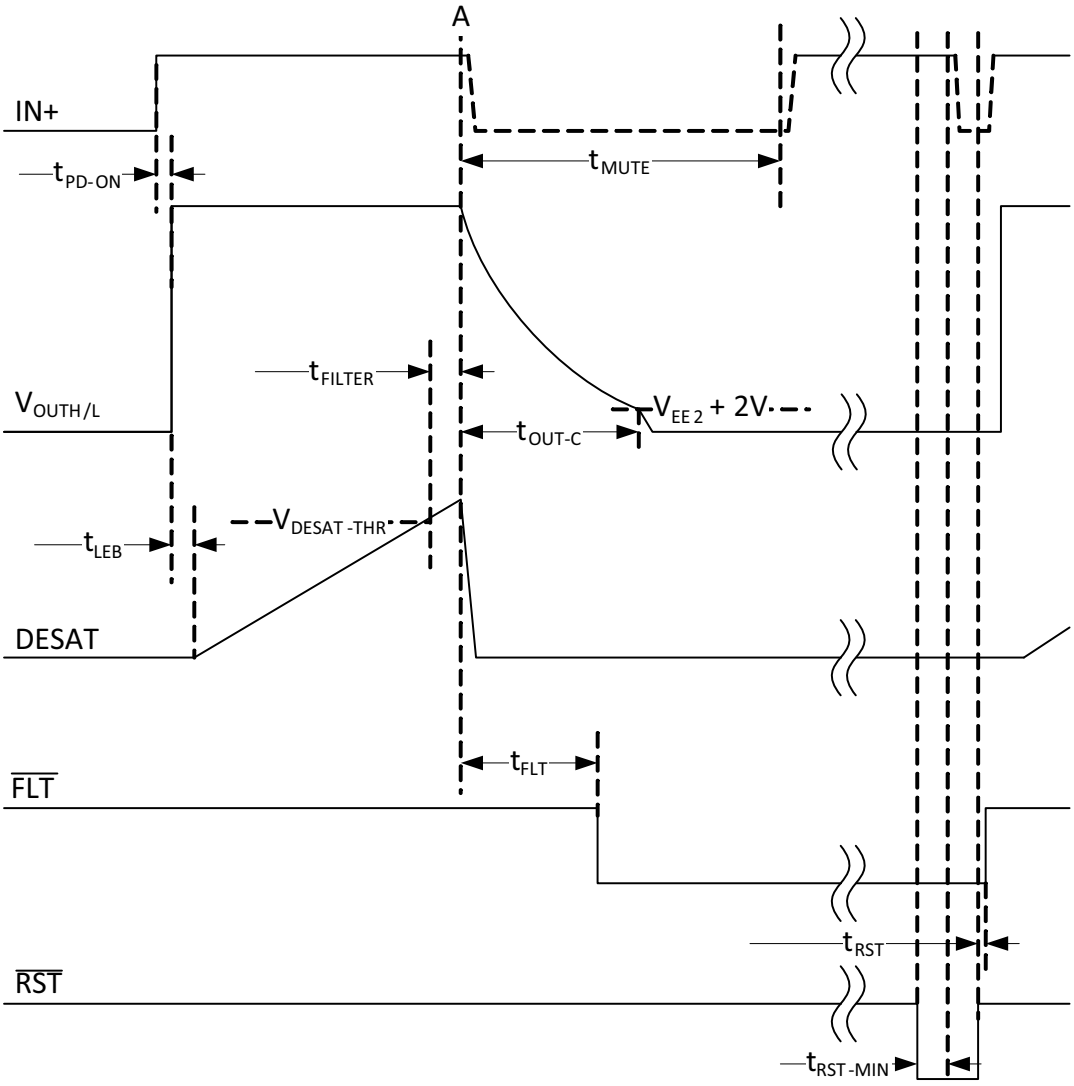



**Figure 23. DESAT Switch Off Behavior**

### Fault Output Pin (FLT)

FLT open−drain output provides feedback to the controller about driver DESAT protection conditions. The open−drain FLT outputs of multiple NCD57001 devices can be wired together forming a single, common fault bus for interfacing directly to the microcontroller. FLT output has 50kΩ internal pull−up resistor to VDD1.

### Ready Output Pin (RDY)

RDY open−drain output provides feedback to the controller about driver UVLO and TSD protections conditions.

- If either side of device have insufficient supply (VDD1 or VDD2), the RDY pin output goes low; otherwise, RDY pin output is open drain.
- If the temperature crosses the TSD threshold, the RDY pin output goes low; otherwise, RDY pin output is open drain.

The open−drain RDY outputs of multiple NCD57001 devices can be “OR”ed together.

### Reset Input Pin (RST)

Reset input pin has internal pull−up resistor to VDD1. In normal condition the RST pin is connected to HIGH, to reset FAULT conditions connect RST pin to LOW. In applications that does not allow to control the reset, RST pin should be connected to IN+, the driver will be reset by each input pulse.

### RESET Input

- FLT input is used to set back FLT output after DESAT conditions disappear

**Warning: When the application use an independent or separate power supply for the control unit ant the input side of the driver, all inputs should be protected by a serial resistor (In case of a power failure of the driver, the driver may be damaged due to overloading of the input protection circuits)**

### Power Supply (VDD1, VDD2, VEE2)

NCD57001 is designed to support two different power supply configurations, bipolar or unipolar power supply. For reliable high output current the suitable external power capacitors required. Parallel combination of 100 nF + 4.7 μF ceramic capacitors is optimal for a wide range of applications using IGBT. For reliable driving IGBT modules (containing several parallel IGBT’s) is a higher capacity required (typically 100 nF + 10 μF). Capacitors should be as close as possible to the driver’s power pins.

- In bipolar power supply the driver is typically supplied with a positive voltage of 15 V at VDD2 and negative voltage −5 V at VEE2 (Figure 24). Negative power supply prevents a dynamic turn on throughout the internal IGBT input capacitance.
- In Unipolar power supply the driver is typically supplied with a positive voltage of 15 V at VDD2. Dynamic turn on throughout the internal IGBT input capacitance could be prevented by Active Miler Clamp function. CLAMP output should be directly connected to IGBT gate (Figure 25).

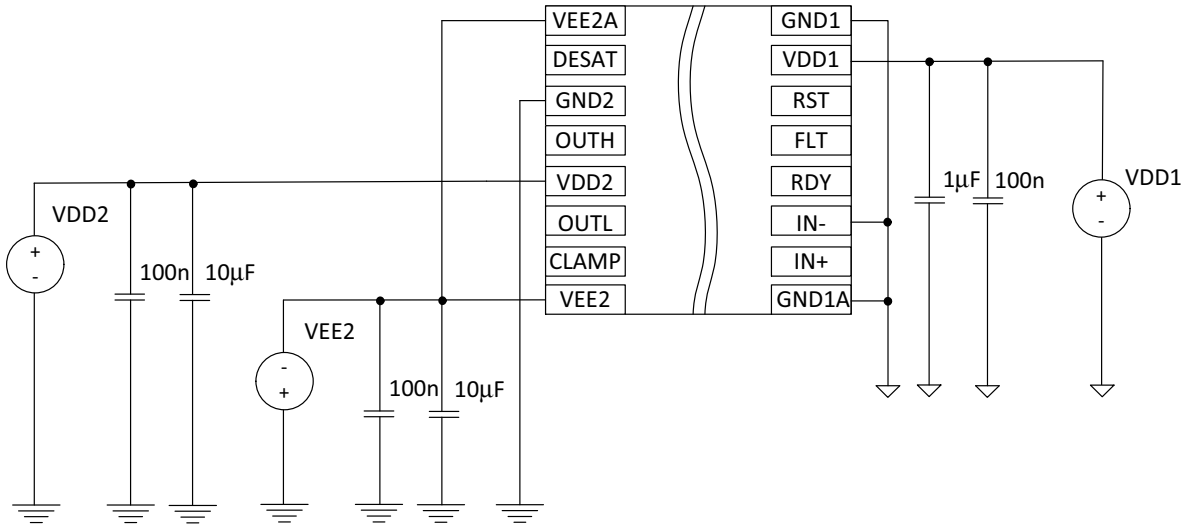



**Figure 24. Bipolar Power Supply**

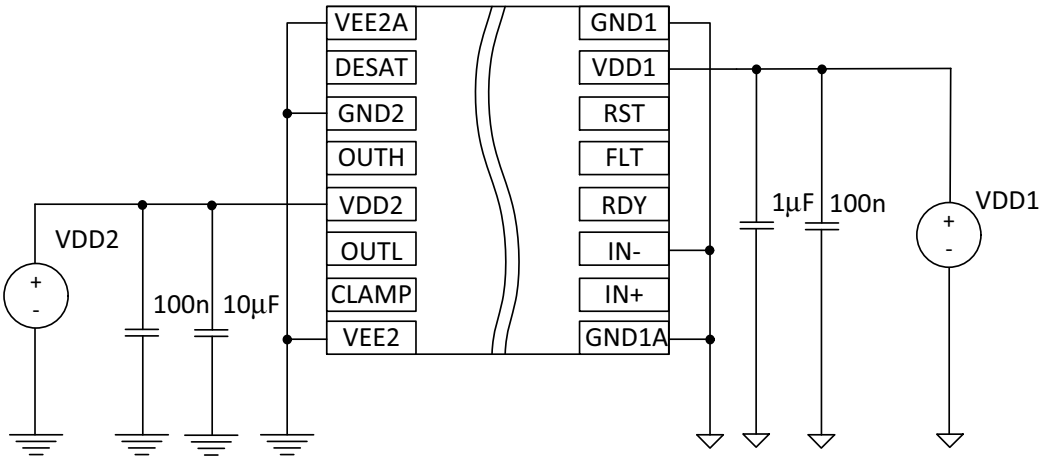



**Figure 25. Unipolar Power Supply**

## Common Mode Transient Immunity (CMTI)

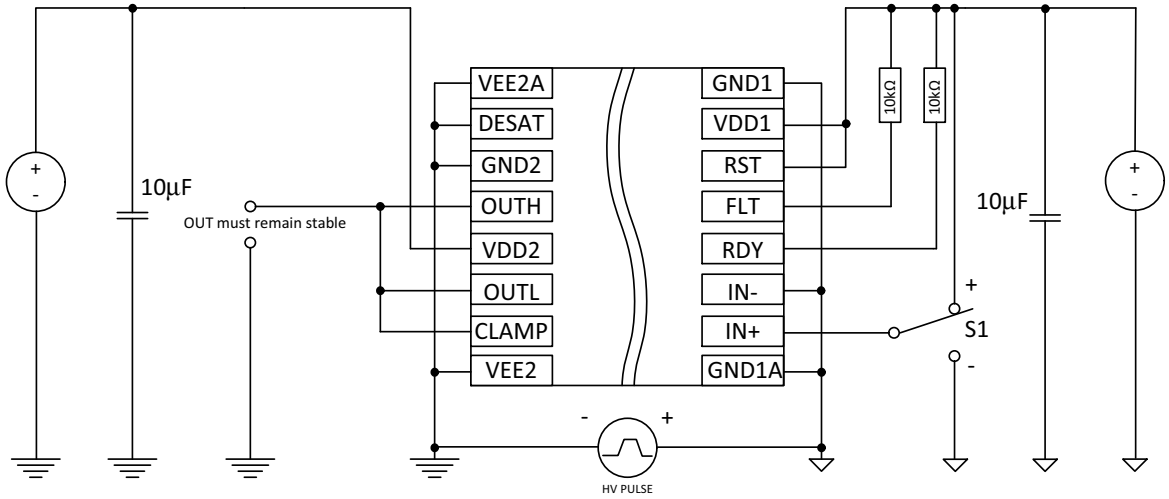



**Figure 26. Common−Mode Transient Immunity Test Circuit**

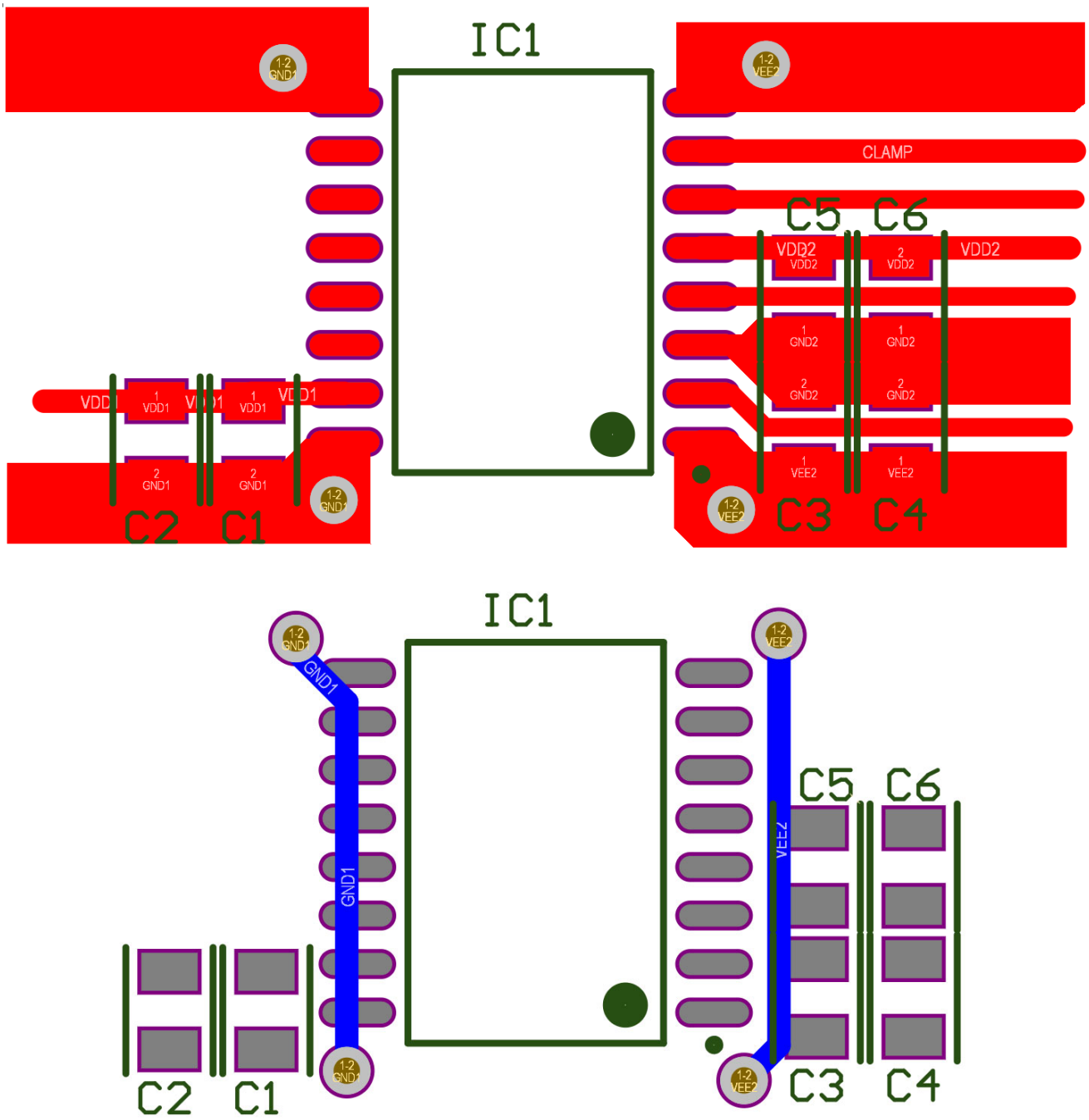



**Figure 27. Recommended Basic Bipolar Power Supply PCB Design**

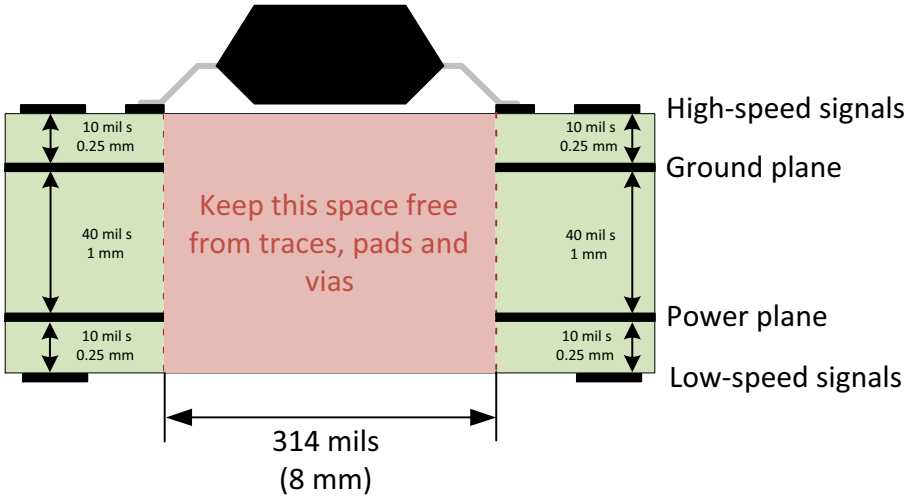
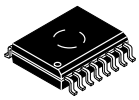



**Figure 28. Recommended Layer Stack**



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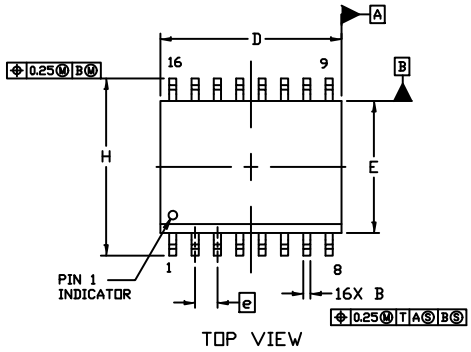
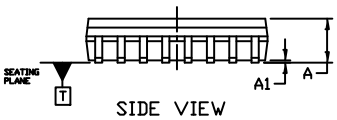
**SCALE 1:1**

**SOIC−16 WB**
CASE 751G
ISSUE E

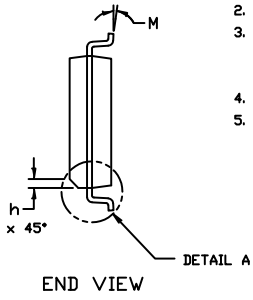
DATE 08 OCT 2021



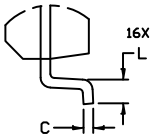

TOP VIEW




SIDE VIEW




END VIEW

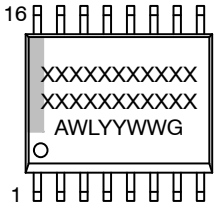



DETAIL A
2X SCALE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

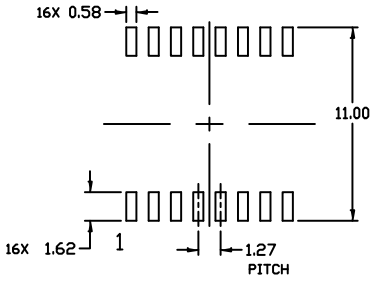
| | MILLIMETERS | |
|---|---|---|
| DIM | MIN. | MAX. |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.53 REF | |
| L | 0.50 | 0.90 |
| M | 0° | 7° |

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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