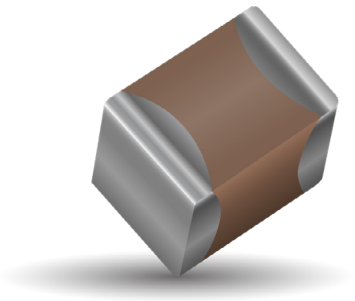
X6S Dielectric, KGM Series

General Specifications



FEATURES

- Offered in a complete range of products for both general and specialized applications and designed to meet a wide variety of needs.
- We have a worldwide network in order to supply our global customer bases quickly and efficiently.
- All ofour products are highly reliable due to their monolithic structure of high-purity and superfine uniform ceramics and their integral internal electrodes.
- By combining superior manufacturing technology and materials with high dielectric constants, we produce extremely compact components with exceptional specifications.
- Our stringent quality control if every phase of production from material procurement to shipping ensures consistent manufacturing and superior quality.

DIELECTRIC CHARACTERISTICS

- Temperature Range: -55 to + 105°C
- Standard Temperature: 25°C
- ΔC Max: ±22%

HOW TO ORDER

KGM	05	H	S6	0G	106	M	N
Series General Purpose Tin/ Nickel Finish	**Size** 03 = 0201 05 = 0402 15 = 0603 21 = 0805	**Thickness** See Cap Chart	**Dielectric** X6S = S6	**Voltage** 0G = 4.0V 0J = 6.3V 1A = 10V 1C = 16V 1E = 25V	**Capacitance Code Code (in pF)** 2 Significant Digits +Number of zeros eg. 10µF = 106 10nF = 103 47pF = 470	**Capacitance Tolerance** K = ±10% M = ±20%	**Packaging** See Table Below

RoHS COMPLIANT

PACKAGING CODES

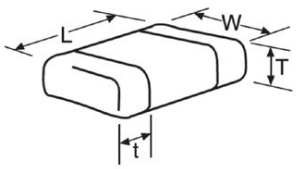
Code	EIA (inch)	IEC(mm)	7" Paper	7" Embossed	13" Paper	13"Embossed
03	0201	0603	H		N	
05	0402	1005	H		N	
15	0603	1608	T		M	
21	0805	2012		U		L

CAPACITANCE RANGE

SIZE		0201			0402		0603					0805				
Packaging		All Paper			All Paper		All Paper					All Embossed				
(L) Length	mm	0.60 ± 0.09			1.00 ±0.20		1.60 ± 0.20					2.01 ± 0.20				
	(in.)	(0.024± 0.004)			(0.040±0.002)		(0.063 ± 0.008)					(0.079 ± 0.008)				
(W) Width	mm	0.30 ±0.09			0.50 ±0.20		0.80 ±0.20					1.25 ± 0.20				
	(in.)	(0.011 ±0.004)			(0.020±0.008)		(0.030 ±0.008)					(0.049 ± 0.008)				
(t) Terminal	mm.	0.18±0.005			0.25±0.10		0.40±0.20					0.50 ± 0.25				
	(in.)	(0.007±0.002)			(0.010±0.004)		(0.016±0.008)					(0.020 ± 0.010)				
WVDC		4	6.3	10	4	6.3	4	6.3	10	16	25	4	6.3	10	16	25
Cap	1.0	C	C	C		A					A					
(µF)	4.7					A		A		C						
	10				H	H		C	C	C	C					F
	22				D		C	C					F	F	F	
	47						C					F				
	100											F				
WVDC		4	6.3	10	4	6.3	4	6.3	10	16	25	4	6.3	10	16	25
Size		0201			0402		0603					0805				

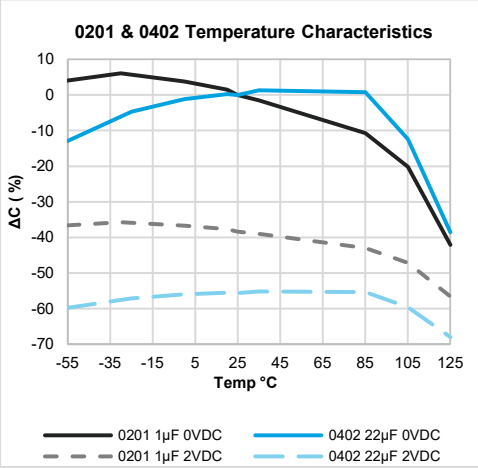
Tan δ Code	Tan δ
7	10.0 % Max.
8	12.5 % Max.
9	15.0 % Max.
10	20.0 % Max.

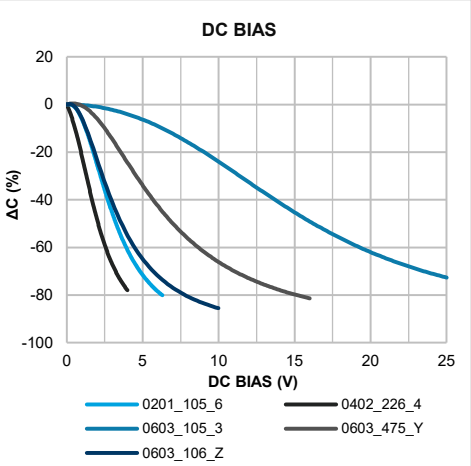
Please Contact for other Tan δ values

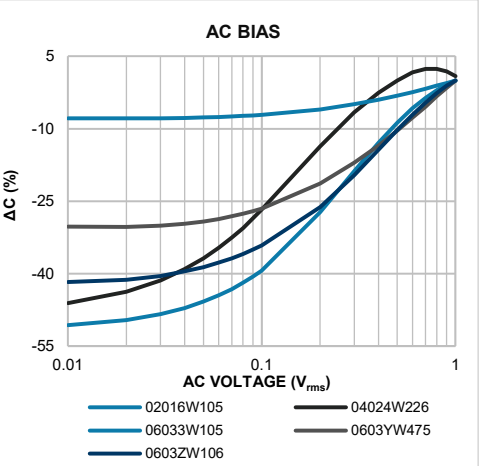


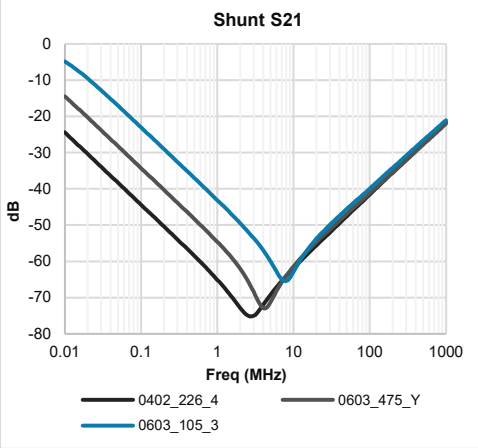
Case Size	0201 (KGM03)	**0402 (KGM05)**			0603 (KGM15)		0805 (KGM21)
Thickness Letter	C	A	D	H	A	C	F
Max Thickness(mm)	0.39	0.55	0.8	0.75	0.9	1	1.52
Carrier Tape	PAPER	PAPER			PAPER		EMB
Packaging Code 7"reel	H	H	H	H	T	T	U
Packaging Code 13"reel	N	N	N	N	M	M	L
	PAPER						Embossed(EMB)

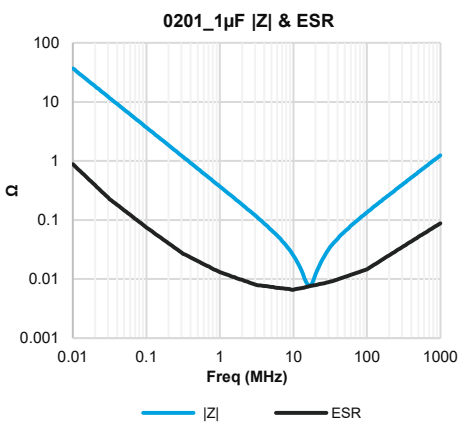
ELECTRICAL CHARACTERISTICS

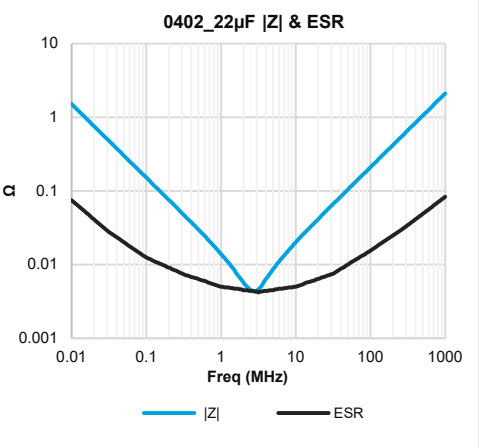


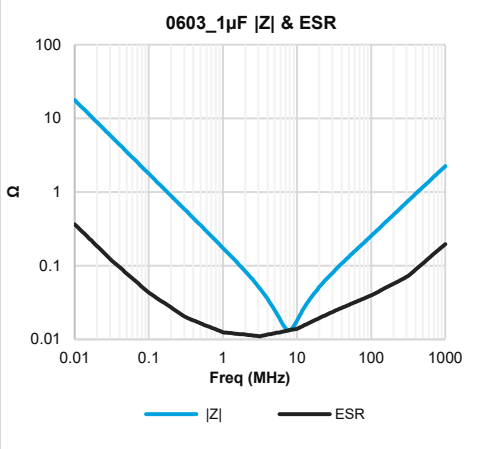


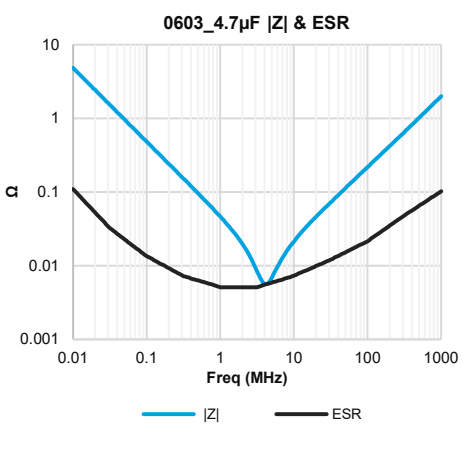


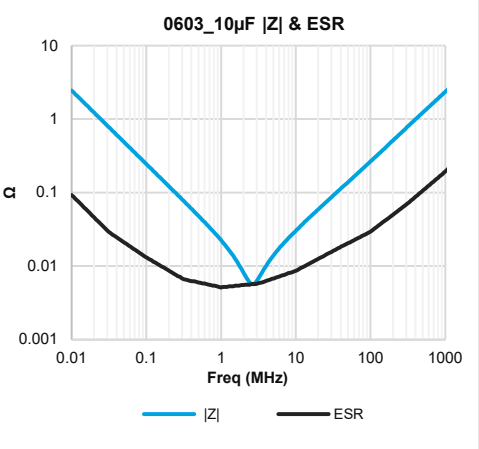












Please Contact for additional characteristics

X6S Dielectric, KGM Series
Specifications and Test Methods

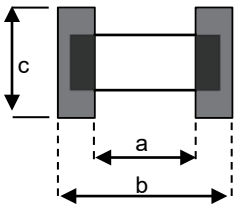
<table>
<tr><th colspan="2">Test Items</th><th>Test Conditions</th><th>Specification</th></tr>
<tr><td colspan="2">Capacitance Value (C)</td><td rowspan="2">Measure after heat treatment
<table><tr><th>Capacitance</th><th>Frequency</th><th>Volt</th></tr><tr><td rowspan="2">C≤10 µF</td><td rowspan="2">1 kHz ±10%</td><td>1.0 ±0.2 V_{rms}</td></tr><tr><td>0.5 ±0.2 V_{rms}</td></tr><tr><td>C>10 µF</td><td>120 Hz ±10%</td><td>0.5 ±0.2 V_{rms}</td></tr></table>The charge and discharge current of the capacitor most not exceed 50mA</td><td>Withen Tolerance</td></tr>
<tr><td colspan="2">Tan δ</td><td>Refer to capacitance chart</td></tr>
<tr><td colspan="2">Insulation Resistance (IR)</td><td>Apply the rated voltage for 1 minute and measure it in normal temperature and humidity. The charge and discharge current of the capacitor must not exceed 50mA.</td><td>Over 50MΩ•µf</td></tr>
<tr><td colspan="2">Dielectric Resistance</td><td>Apply 2.5 times the rated voltage for 1-5 seconds. The charge and discharge current of the capacitor must not exceed 50mA.</td><td>No Defects</td></tr>
<tr><td colspan="2">Appearance</td><td>Microscope</td><td>No problem observed</td></tr>
<tr><td colspan="2">Termination Strength</td><td>Apply a sideward force of 500g (5N) to PCB-mounted sample.</td><td>No Defects</td></tr>
<tr><td colspan="2">Bending Strength</td><td>Glass epoxy PCB: Fulcrum spacing: 90mm, duration time 10 seconds.</td><td>No Significant damage with 1mm bending.</td></tr>
<tr><td rowspan="3">Vibration Test</td><td>Appearance</td><td rowspan="3">Take the initial value after heat treatment.Vibration Frequency: 10-55 (Hz)Amplitude: 1.5mmSweeping Condition: 10 → 55 → 10 Hz/ 1 minute in X, Y and ZDirections: 2 hours each, 6 hours total, and place in normal temperature and humidity. Measure the sample after heat treatment.</td><td>No problem observed</td></tr>
<tr><td>Δ C</td><td>Within Tolerance</td></tr>
<tr><td>Tan δ</td><td>Within Tolerance</td></tr>
<tr><td rowspan="5">Soldering Heat Resistant</td><td>Appearance</td><td rowspan="5">Take the initial value after heat treatment.Soak the Sample in 260°C ±5°C solder for 10±0.5 seconds and place in normal temperature and humidity. Measure after heat treatment.(Pre-heating conditions)
<table><tr><th>Capacitance</th><th>Frequency</th><th>Volt</th></tr><tr><td>1</td><td>80-100°C</td><td>2 min</td></tr><tr><td>2</td><td>150-200°C</td><td>2 min</td></tr></table>The charge and discharge current of the capacitor must not exceed 50mA for IR and Withstanding Voltage measurement.</td><td>No Defects</td></tr>
<tr><td>Δ C</td><td>Within ±7.5%</td></tr>
<tr><td>Tan δ</td><td>Within Tolerance</td></tr>
<tr><td>IR</td><td>Over 50MΩ•µF</td></tr>
<tr><td>Withstanding Voltage</td><td>Resist without problem</td></tr>
<tr><td colspan="2">Solderability</td><td>Soak Condition:
<table><tr><td>Sn-3AG-0.5Cu</td><td>245 ± 5°C</td><td>3 ±0.5 sec.</td></tr><tr><td>Sn63 Solder</td><td>235 ± 5°C</td><td>2 ±0.5 sec.</td></tr></table></td><td>Solder Coverage : 90% min.</td></tr>
<tr><td rowspan="5">Temperature Cycle</td><td>Appearance</td><td rowspan="5">Take initial value after heat treatment.
(Cycle)
Room Temperature (3min.) → Lowest Operating Temperature (30 min.) → Room Temperature (3 min.) → Highest Operating Temperature (30 min.) After 5 cycles, measure after heat treatment.The charge and discharge current of the capacitor must not exceed 50mA for IR and Withstanding Voltage measurement.</td><td>No Defects</td></tr>
<tr><td>Δ C</td><td>Within ±7.5%</td></tr>
<tr><td>Tan δ</td><td>Within Tolerance</td></tr>
<tr><td>IR</td><td>Over 50MΩ•µF</td></tr>
<tr><td>Withstanding Voltage</td><td>Resist without problem</td></tr>
<tr><td rowspan="4">Moisture Resistant Load</td><td>Appearance</td><td rowspan="4">Take the initial value after heat treatment.After applying the rated voltage for 500-512 hours in the condition of 40°C±2°C and 90 to 95% RH, place in normal temperature and humidity, then measure the sample after heat treatment.The charge and discharge current of the capacitor must not exceed 50mA for IR measurement</td><td>No Defects</td></tr>
<tr><td>Δ C</td><td>Within ±12.5%</td></tr>
<tr><td>Tan δ</td><td>200% max. of initial value</td></tr>
<tr><td>IR</td><td>Over 10MΩ•µF</td></tr>
<tr><td rowspan="4">High-Temperature Load</td><td>Appearance</td><td rowspan="4">Take the initial value after heat treatment.After applying *twice the rated voltage in the highest operating temperature for 1000-1012 hours, measure the sample after heat treatment in normal temperature and humidity. The charge and discharge current of the capacitor must not exceed 50mA for IR measurement.</td><td>No Defects</td></tr>
<tr><td>Δ C</td><td>Within ±12.5%</td></tr>
<tr><td>Tan δ</td><td>200% max. of initial value</td></tr>
<tr><td>IR</td><td>Over 10MΩ•µF</td></tr>
</table>

Heat Treatment	Expose sample to temperature of 140-150°C for 1 hour and leave the sample in normal temperature and humidity for 24 ±2 hours.

*Apply 1 times when the rated voltage is 4V or less

Please contact KYOCERA AVX for the optional specification of the capacitance chart.

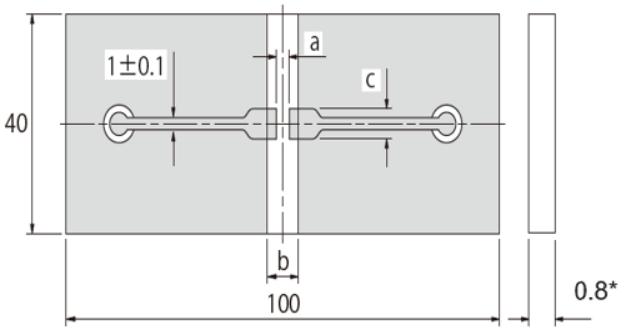
Substrate for Adhesion Strength Test, Vibration Test, Soldering Heat Resistance Test, Temperature Cycle Test, Load Humidity Test, High-Temperature with Loading Test.

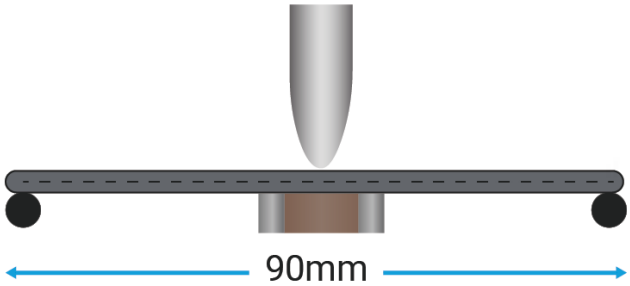


units: mm

Size (EIA Code)	a	b	c
0201	0.26	0.92	0.32
0402	0.4	1.4	0.5
0603	1.0	3.0	1.2

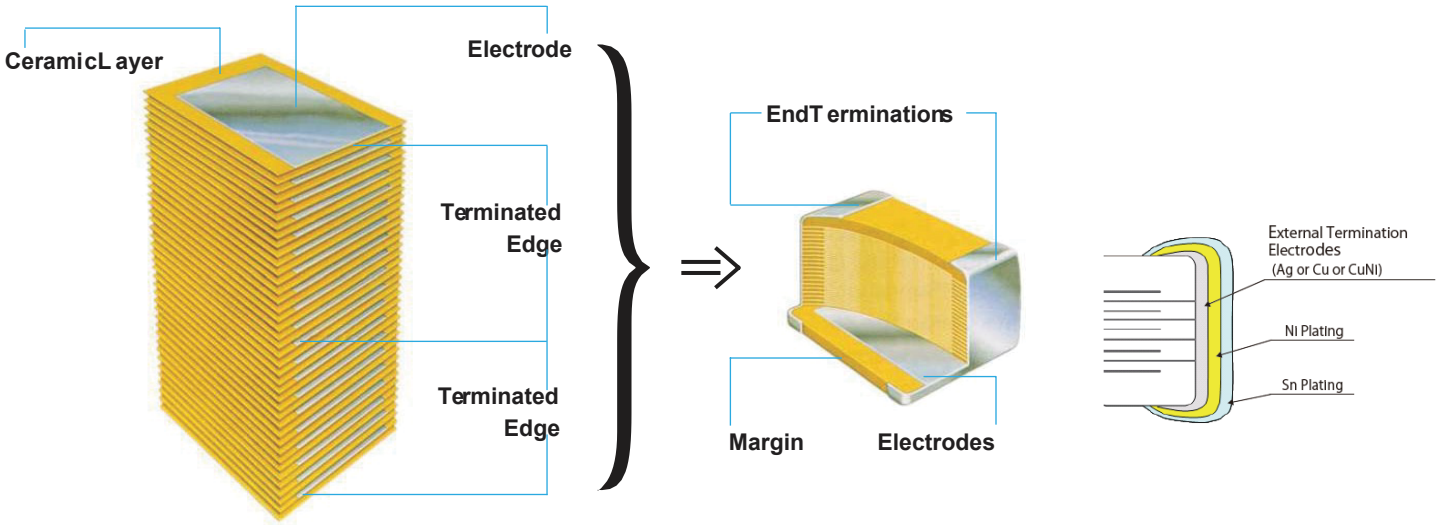
SUBSTRATE FOR BENDING TEST Unit: mm





TestingB oard:G lass EpoxyB oard (CE4 or FR4)
TestingB oard Thickness: 0.8 ±0 .1mm*
CircuitT hickness: 0.04 ±0 .01mm

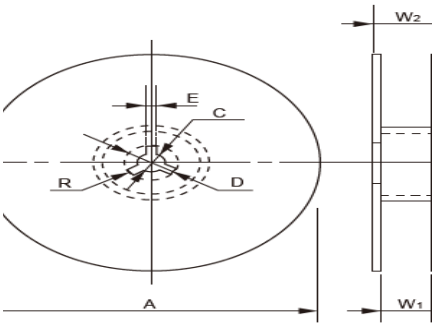
STRUCTURE



- Please contact your local AVX Sales office or distributor for specifications not covered in this catalog.
- Capacitance range is subject to change without notice

Please contact sales representative to confirm compatibility with your application.

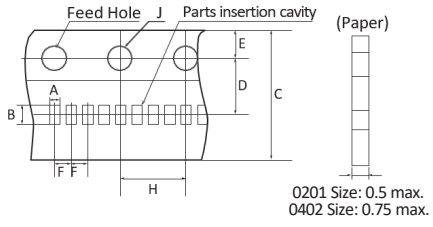
TAPE & REEL QUANTITIES



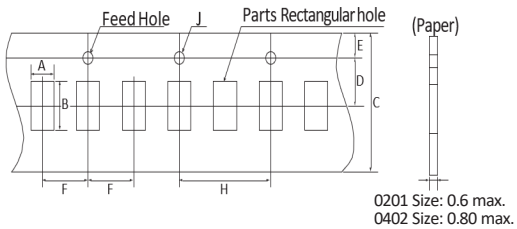
Code Reel	A	B	C	D	E	W_1	W_2	R
7-inch Reel	180 $^{+0}_{-2.0}$	Φ60 min.	13±0.5	21±0.8	2.0±0.5	10.5±1.5	16.5 max.	1.0

CARRIER TAPE

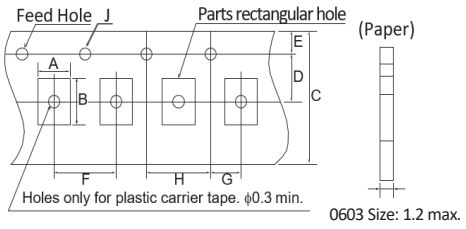
F= 1mm (0201 & 0402)



F= 2mm (0201 & 0402)



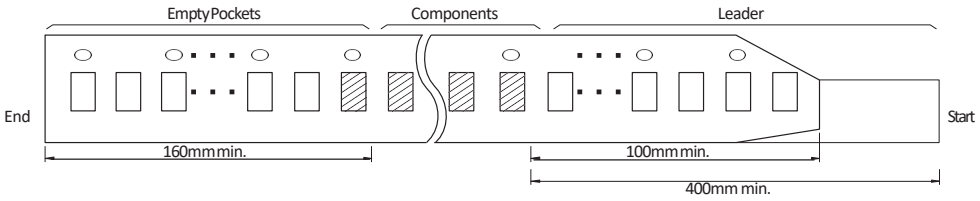
F= 4mm (0603)



Units: mm

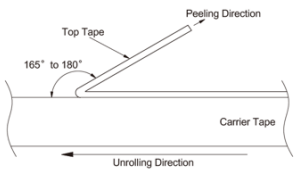
Size	A	B	C	D	E	F	G	H	J	Carrier Width
0201	0.37 ± 0.03	0.67 ± 0.03	8.0 +0.3/ -0.1	3.5 ± 0.05	1.75 ± 0.1	1.0 ± 0.05	-	4.0 ± 0.05	1.5 + 0.1	8mm
	0.39 ± 0.03	0.69 ± 0.03	8.0 ± 0.3			2.0 ± 0.05		4.0 ± 0.1		
	0.42 ± 0.03	0.72 ± 0.03								
0402	0.65 ± 0.1	1.15 ± 0.1	8.0 +0.3/ -0.1	3.5 ± 0.05	1.75 ± 0.1	1.0 ± 0.05	-	4.0 ± 0.05	1.5 + 0.1	8mm
	0.75 ± 0.1		8.0 ± 0.3			2.0 ± 0.05		4.0 ± 0.1		
	0.8 ± 0.1	1.3 ± 0.1								
0603	1.0 ± 0.2	1.8 ± 0.2	8.0 ± 0.3	3.5 ± 0.05	1.75 ± 0.1	4.0± 0.1	2.0 ± 0.05	4.0 ± 0.1	1.5 + 0.1	8mm
	1.1 ± 0.2	1.9 ± 0.2								

DETAIL OF LEADER AND TRAIL



ADHESIVE TAPE

- The exfoliative strength when peeling off the top tape from the carrier tape by the method of the following figure shall be *0.1 to 0.5N.
- When the top tape is peeled off, the adhesive stays on the top tape.
- Chip capacitors will be in a state free without being stuck on the thermal adhesive tape.2

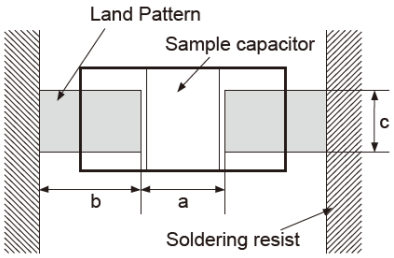


CARRIER TAPE

- Chip will not fall off from carrier tape or carrier tape will not be damaged by bending than within a radius of 25mm.
- The chip are inserted continuously without any empty pocket.
- Chip will not be mis-mounted because of too big clearance between components and cavity. Also the waste of carrier tape will not fill a nozzle hole of mounting machine.

DIMENSIONS FOR RECOMMENDED TYPICAL LAND

Since the amount of solder (size of fillet) to be used has direct influence on the capacitor after mounting, the sufficient consideration is necessary. When the amounts of solder is too much, the stress that a capacitor receives becomes larger. It may become the cause of a crack in the capacitor. When the land design of printed wiring board is considered, it is necessary to set up the form and size of land pattern so that the amount of solder is suitable.



GENERAL Unit: mm

Size (EIA Code)	Dimension		Recommended Land Dimesnions		
	L	W	a	b	c
0201	0.6 ± 0.03	0.3 ± 0.03	0.20 to 0.25	0.25 to 0.35	0.30 to 0.40
	0.6 ± 0.5	0.3 ± 0.05			
	0.6 ± 0.09	0.3 ± 0.09	0.23 to 0.30		0.30 to 0.45
0402	1.0 ± 0.05	0.5 ± 0.05	0.30 to 0.50	0.35 to 0.45	0.40 to 0.60
	1.0 ± 0.15	0.5 ± 0.15	0.40 to 0.60	0.40 to 0.50	0.50 to 0.75
	1.0 ± 0.20	0.5 ± 0.20			
0603	1.6 ± 0.10	0.8 ± 0.10	0.70 to 1.00	0.80 to 1.00	0.60 to 0.90
	1.6 ± 0.15	0.8 ± 0.15	0.80 to 1.00		0.80 to 1.10
	1.6 ± 0.20	0.8 ± 0.20			
	1.6 ± 0.25	0.8 ± 0.25			

* Recommended land dimensions may differ depending on dimensional tolerance

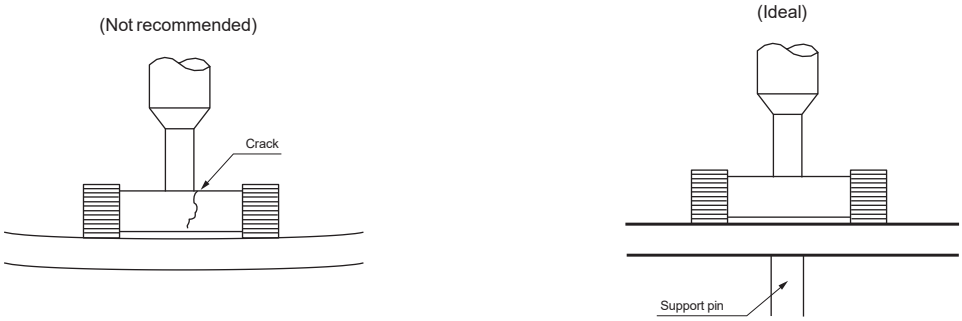
MOUNTING DESIGN

The chip could crack if the PCB warps during processing after the chip has been soldered.

Recommended chip position on PCB to minimize stress from PCB warpage

MOUNTING

1. If the position of the vacuum nozzle is too low, a large force may be applied to the chip capacitor during mounting, resulting in cracking.
2. During mounting, set the nozzle pressure to a static load of 1 to 3 N.
3. To minimize the shock of the vacuum nozzle, provide a support pin on the back of the PCB to minimize PCB flexure.



4. Bottom position of pick-up nozzle should be adjusted to the top surface of a substrate when camber is corrected

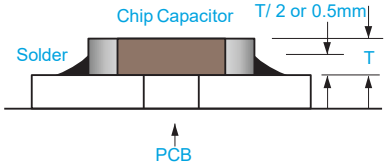
RESIN MOLD

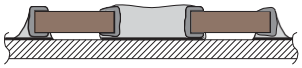
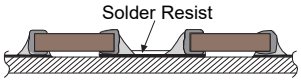
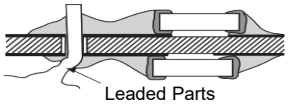
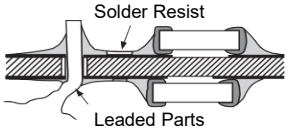
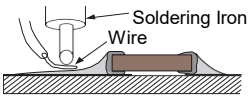
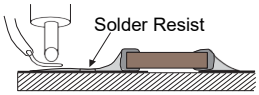
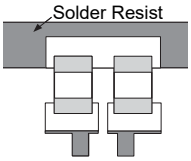
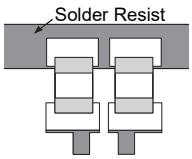
- If a large amount of resin is used for molding the chip, cracks may occur due to contraction stress during curing. To avoid such cracks, use a low shrinkage resin.
- The insulation resistance of the chip will degrade due to moisture absorption. Use a low moisture absorption resin.
- Check carefully that the resin does not generate a decomposition gas or reaction gas during the curing process or during normal storage. Such gases may crack the chip capacitor or damage the device itself.

DESIGN OF PRINTED CIRCUIT AND SOLDERING

The recommended fillet height shall be 1/2 of the thickness of capacitors or 0.5mm. When mounting two or more capacitors in the common land, it is necessary to separate the land with the solder resist strike so that it may become the exclusive land of each capacitor.

IDEAL SOLDER HEIGHT



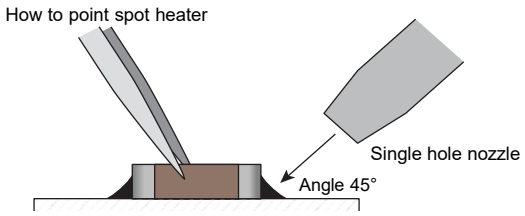
Item	Prohibited	Rexommended Example : Separation by Solder Resist
Multiple Parts Mount		
Mount With Leaded Parts		
Wire Soldering After Mounting		
Side by Side Layout		

SOLDERING METHOD

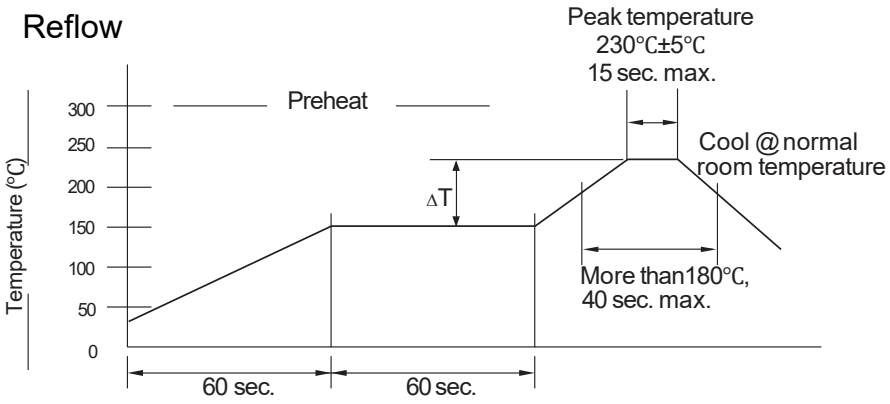
1. Ceramic is easily damaged by rapid heating or cooling. If some heat shock is unavoidable, preheat enough to limit the temperature difference (Delta T) to within 150°C
2. The product size 1.6×0.8mm to 3.2×1.6mm can be used in reflow and wave soldering, and the product size of bigger than 3.2×1.6mm, or smaller than 1.6 × 0.8mm can be used in reflow. Circuit shortage and smoking can be created by using capacitors which are used neglecting the above caution
3. Please see our recommended soldering conditions
4. In case of using Sn-Zn Solder, please contact us in advance
5. The following condition is recommended for spot heater application

RECOMMENDED SPOT HEATER CONDITION

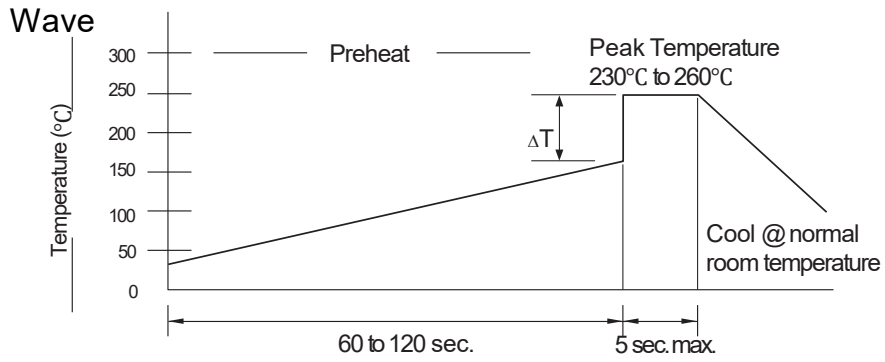
Item	Condition
Distance	5mm min.
Angle	45°
Projection Temp.	400℃
Flow Rate	Set at the minimum
Nozzle Diameter	2ϕ to 4ϕ (Single hole type)
Applucation Time	10 sec max.



RECOMMENDED TEMPERATURE PROFILE (Sn-3Ag-0.5Cu)

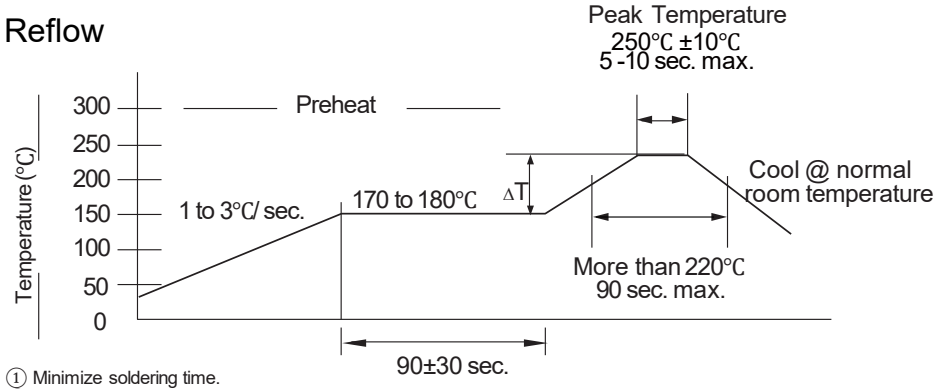


① Minimize soldering time.
② Ensure that the temperature difference (ΔT) does not exceed 150°C.
③ Ensure that the temperature difference (ΔT) does not exceed 130°C for 3.2×2.5mm size or larger.
④ MLCC can withstand the above reflow conditions up to 3 times.

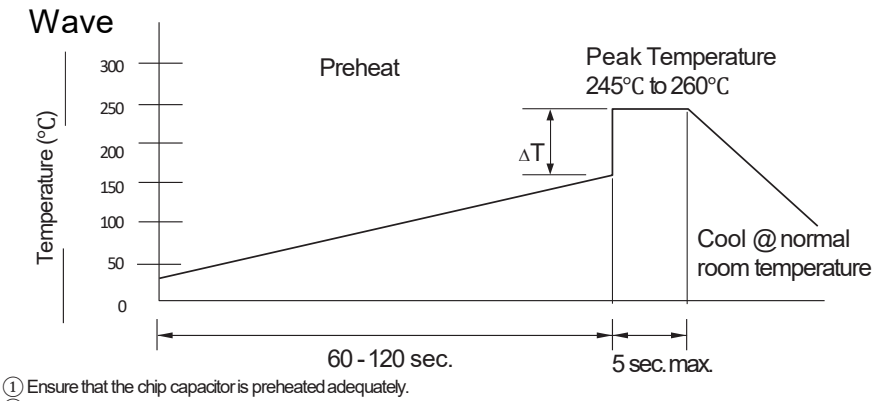


① Ensure that the chip capacitor is preheated adequately.
② Ensure that the temperature difference (ΔT) does not exceed 150°C.
③ Cool naturally after soldering.
④ Wave soldering is not applicable for chips with size of 3.2×2.5mm or larger of 1.0×0.5mm or smaller and capacitor arrays.

RECOMMENDED TEMPERATURE (63n Solder)



① Minimize soldering time.
② Ensure that allowable temperature difference does not exceed 150°C.
③ Ensure that allowable temperature difference does not exceed 130°C for 3.2×2.5mm size or larger.
④ MLCC can withstand the above reflow conditions up to 3 times.
⑤ N_2 atmosphere is recommended for reflow of products of 0.4mm×0.2mm size or smaller.



① Ensure that the chip capacitor is preheated adequately.
② Ensure that the temperature difference (ΔT) does not exceed 150°C.
③ Cool naturally after soldering.
④ Wave soldering is not applicable for chips with size of 3.2×2.5mm or larger of 1.0×0.5mm or smaller and capacitor arrays.

CIRCUIT DESIGN

1. Once application and assembly environments have been checked, the capacitor may be used in conformance with the rating and performance which are provided in both the catalog and the specifications. Use exceeding that which is specified may result in inferior performance or cause a short, open, smoking, or flaming to occur, etc.

2. Please consult the manufacturer in advance when the capacitor is used in devices such as: devices which deal with human life, i.e. medical devices; devices which are highly public orientated; and devices which demand a high standard of liability. Accident or malfunction of devices such as medical devices, space equipment and devices having to do with atomic power could generate grave consequence with respect to human lives or, possibly, a portion of the public. Capacitors used in these devices may require high reliability design different from that of general-purpose capacitors.

3. Please use the capacitors in conformance with the operating temperature provided in both the catalog and the specifications. Be especially cautious not to exceed the maximum temperature. In the situation the maximum temperature set forth in both the catalog and specifications is exceeded, the capacitor's insulation resistance may deteriorate, power may suddenly surge and short-circuit may occur. The capacitor has a loss and may self-heat due to equivalent series resistance when alternating electric current is passed therethrough. As this effect becomes especially pronounced in high frequency circuits, please exercise caution. When using the capacitor in a (self-heating) circuit, please make sure the surface of the capacitor remains under the maximum temperature for usage. Also, please make certain temperature rises remain below 20℃ .

4. Please keep voltage under the rated voltage which is applied to the capacitor. Also, please make certain the peak voltage remains below the rated voltage when AC voltage is super-imposed to the DC voltage. In the situation where AC or pulse voltage is employed, ensure average peak voltage does not exceed the rated voltage. Exceeding the rated voltage provided in both catalog and specifications may lead to defective withstanding voltage or, in worst case situations, may cause the capacitor to smoke or flame.

5. When the capacitor is to be employed in a circuit in which there is continuous application of a high frequency voltage or a steep pulse voltage, even though it is within the rated voltage, please inquire to the manufacturer. In the situation the capacitor is to be employed using a high frequency AC voltage or an extremely fast rising pulse voltage, even though it is within the rated voltage, it is possible capacitor reliability will deteriorate.

6. It is a common phenomenon of high-dielectric products to have a deteriorated amount of static electricity due to the application of DC voltage. Due caution is necessary as the degree of deterioration varies depending on the quality of capacitor materials, capacity, as well as the load voltage at the time of operation.

7. Do not use the capacitor in an environment where it might easily exceed the respective provisions concerning shock and vibration specified in the catalog and specifications. In addition, it is a common piezo phenomenon of high dielectric products to have some voltage due to vibration or to have noise due to voltage change. Please contact sales in such case.

8. If the electrostatic capacity value of the delivered capacitor is within the specified tolerance, please consider this when designing the respective product in order that the assembled product function appropriately.

9. Please contact us upon using conductive adhesives.

STORAGE

1. If the component is stored in minimal packaging (a heat-sealed or zippered plastic bag), the bag should be kept closed. Once the bag has been opened, reseal it or store it in a desiccator.

2. Keep storage place temperature + 5 to + 40 ℃ , humidity 20 to 70% RH. See JIS C 6 0721-3-1, class 1K2 for other climatic conditions.

3. The storage atmosphere must be free of corrosive gas such as sulfur dioxide and chlorine. Also, avoid exposing the product to saline moisture. If the product is exposed to such atmospheres, the terminals will oxidize and solderability will be affected.

4. Precautions 1) to 3) apply to chip capacitors packaged in carrier tapes.

5. The solderability is assured for 6 months from our shipping date if the above storage precautions are followed.