AsahiKASEI MICRODEVICES

AK4438

108dB 768kHz 32bit 8-Channel Audio DAC

1. General Description

The AK4438 is an 8-channel 32-bit DAC which corresponds to digital audio systems. sound. It supports PCM input up to 768kHz sampling rate, suitable for play backing high resolution audio sources that are becoming widespread in network audios, USB-DACs and Car Audio Systems. In addition, “OSR-Doubler” technology is adopted, making the AK4438 capable of supporting wide range signals and achieving low out-of-band noise while realizing low power consumption. Moreover, the AK4438 has five types of short group delay and high sound quality 32-bit digital filters, realizing simple and flexible sound making in wide range of applications.

Application: AV Receivers, CD/SACD Players, Network Audios, USB DACs, USB Headphones, Sound Plate/Bars, Car Audios, Automotive External Amplifiers, Measuring Instruments and Control Systems.

2. Features

1. **8-ch 32-bit DAC**
   - **256× Over Sampling**
   - **32-bit High Quality Sound Short Delay Digital Filter**
   - **Single-ended Output, Smoothing Filter**
   - **THD+N: 91 dB**
   - **DR, S/N: 108 dB**
   - **Channel Independent Digital Volume (0 dB to −127 dB, 0.5 dB Step and Mute)**
   - **Soft Mute**
   - **De-emphasis Filter (supporting 32kHz, 44.1kHz and 48kHz)**
   - **I/F Format: MSB justified, LSB justified, I^2S, TDM**
   - **Zero Detection**
2. **Sampling Frequency**
   - **Normal Speed mode: 8 kHz to 48 kHz**
   - **Double Speed mode: 48 kHz to 96 kHz**
   - **Quad Speed mode: 96 kHz to 192 kHz**
   - **Oct Speed mode: 384 kHz**
   - **Hex Speed mode: 768 kHz**
3. **Master Clock**
   - **256fs, 384fs, 512fs, 768fs (Normal Speed mode: fs = 8 kHz to 48 kHz)**
   - **256fs, 384fs (Double Speed mode: fs = 48 kHz to 96 kHz)**
   - **128fs, 192fs (Quad Speed mode: fs = 96 kHz to 192 kHz)**
   - **64fs, 96fs (Oct Speed mode: fs = 384 kHz)**
   - **32fs, 48fs (Hex Speed mode: fs = 768 kHz)**
4. **µP Interface: 3-wire Serial/ I^2C bus (Fast mode: 400 kHz)**
5. **Power Supply**
   - **Analog Supply: AVDD = 3.0 V to 3.6 V**
   - **In/Output Buffer Supply: TVDD = 1.7 V to 3.6 V**
   - **Integrated LDO for Digital Power Supply**
6. **Current Consumption: 31 mA (fs = 48 kHz)**
7. **Operating Temperature: Ta = −40 °C to 105 °C**
8. **Package: 32-pin QFN (0.5 mm pitch)**

3. Table of Contents

4. Block Diagram

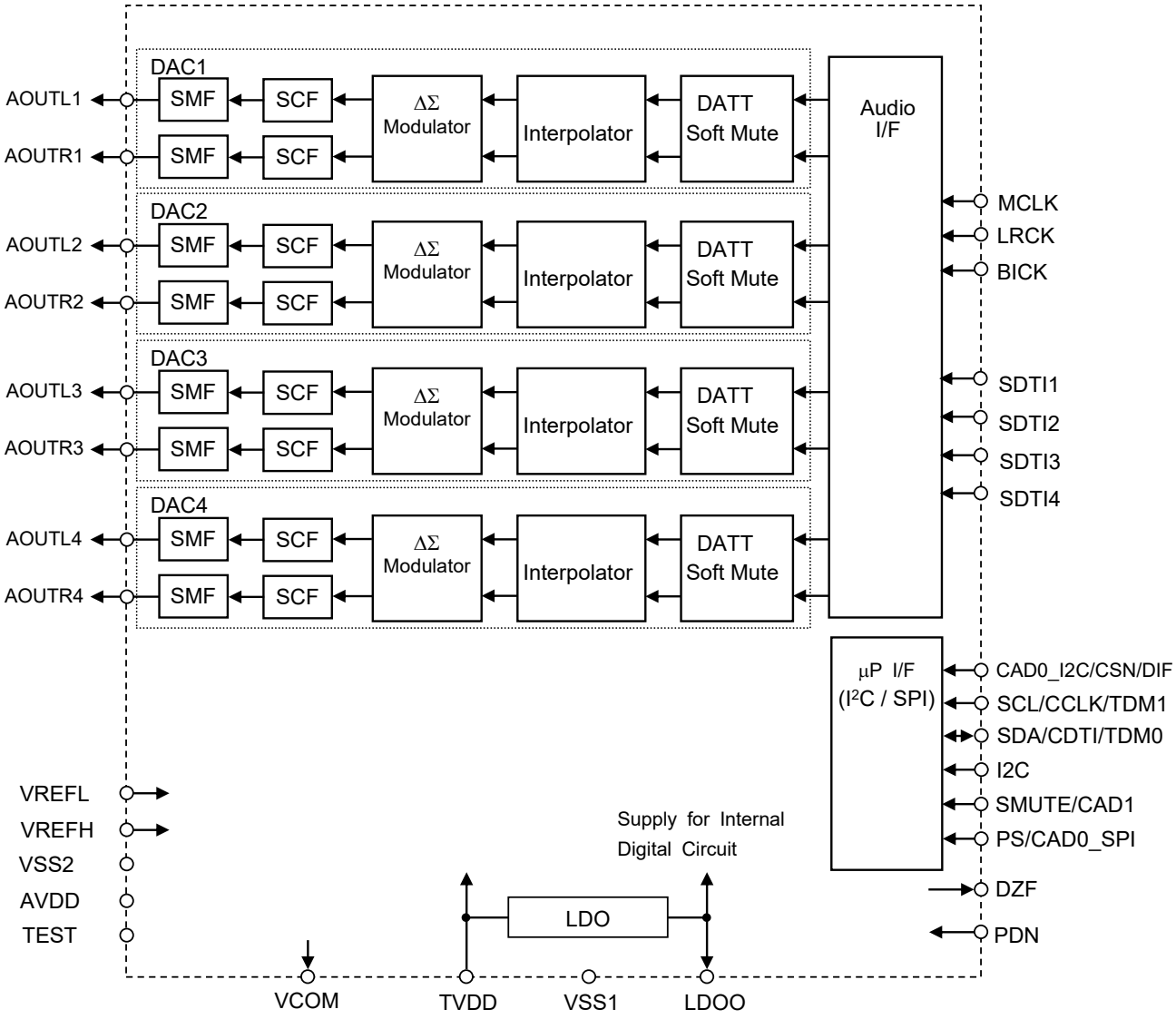


Figure 1. Block Diagram

Block	Function
Audio I/F	Converts audio serial data input from SDTI1–4 pins using LRCK and BICK to parallel data for internal use.
DATT, Soft Mute	Adjusting the amplitude of audio data and controlling soft mute operation
Interpolator	Digital filter that oversamples audio data
ΔΣ Modulator	Third-order digital delta-sigma modulator for noise shaping
SCF	A first-order switched capacitor filter that converts the ΔΣ modulator output into an analog signal
SMF	A smoothing filter that removes high frequency noise remaining in the analog signal output from the SCF.
μP I/F (I²C / SPI)	Control registers and interfaces for setting various operating modes
LDO	Generates power supply (1.2 V typ) for internal digital circuits

5. Pin Configration and Functions

5.1. Pin Configuration

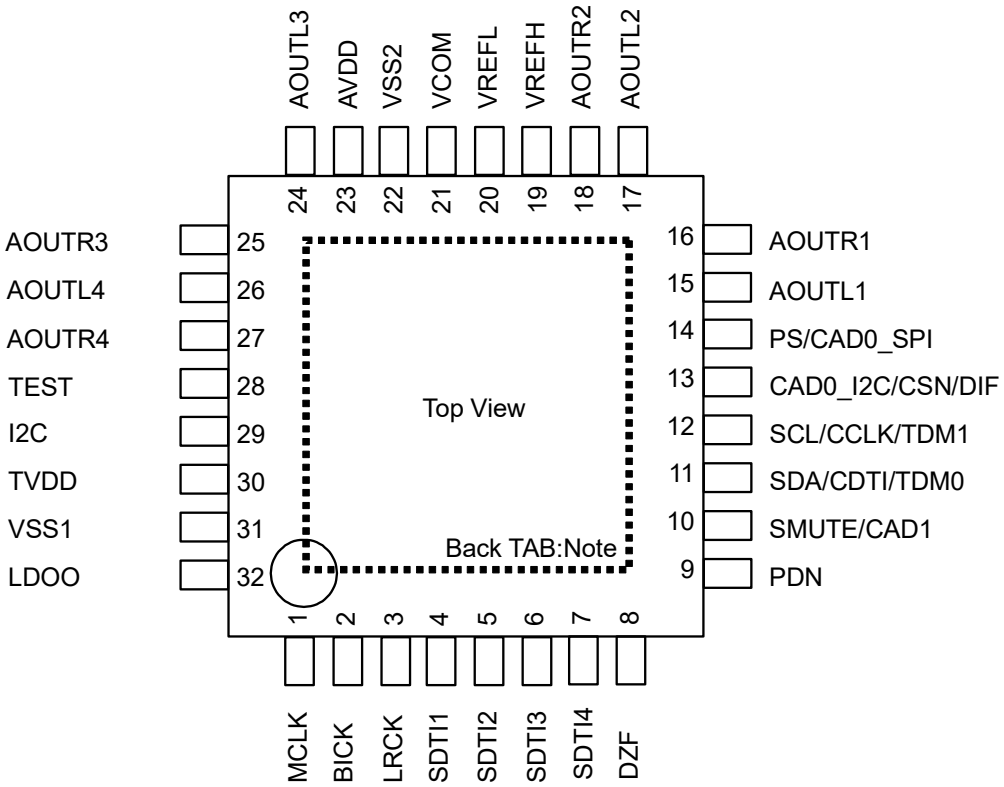


Figure 2. Pin Configuration

Note: The exposed pad on the bottom surface of the package must be open or connected to the analog ground

5.2. Pin Functions

No.	Pin Name	I/O	State at Power Down	Function
1	MCLK	I	Hi-z	External Master Clock Input Pin
2	BICK	I	Hi-z	Audio Serial Data Clock Input Pin
3	LRCK	I	Hi-z	Channel Clock Input Pin
4	SDTI1	I	Hi-z	Audio Serial Data Input Pin
5	SDTI2	I	Hi-z	Audio Serial Data Input Pin
6	SDTI3	I	Hi-z	Audio Serial Data Input Pin
7	SDTI4	I	Hi-z	Audio Serial Data Input Pin
8	DZF	O	50 kΩ Pull-down	Zero Detect Flag Output Pin The function is available in I²C Bus or 3-wire serial control mode.
9	PDN	I	Hi-z	Power-Down & Reset Pin. When "L", the AK4438 is powered-down and the control registers are reset to default state.
10	SMUTE	I	Hi-z	Soft Mute Pin in Parallel control mode. When this pin is changed to "H", soft mute cycle is initiated. When returning "L", the output mute releases.
	CAD1	I		Chip Address 1 Pin in I²C Bus or 3-wire Serial Control mode
11	SDA	I/O	Hi-z	Control Data Input Pin in I²C Bus Control mode
	CDTI	I		Control Data Input Pin in 3-wire Serial Control mode
	TDM0	I		TDM Mode select pin in Parallel Control mode.
12	SCL	I	Hi-z	Control Data Clock Pin in I²C Bus Control mode
	CCLK	I		Control Data Clock Pin in 3-wire Serial Control mode
	TDM1	I		TDM Mode Select Pin in Parallel Control mode.
13	CAD0_I2C	I	Hi-z	Chip Address 0 Pin in I²C Bus Control mode
	CSN	I		Chip Select Pin in 3-wire Serial Control mode
	DIF	I		Audio Data Format Select in Parallel Control mode. "L": 32-bit MSB, "H": 32-bit I²S
14	PS	I	Hi-z	(I2C pin = "H") Control Mode Select Pin "L": I²C Bus Control mode, "H": Parallel Control mode.
	CAD0_SPI	I		(I2C pin = "L") Chip Address 0 Pin in 3-wire Serial Control mode
15	AOUTL1	O	Hi-z	Lch Analog Output Pin
16	AOUTR1	O	Hi-z	Rch Analog Output Pin
17	AOUTL2	O	Hi-z	Lch Analog Output Pin
18	AOUTR2	O	Hi-z	Rch Analog Output Pin
19	VREFH	I	Hi-z	Positive Voltage Reference Input Pin, AVDD
20	VREFL	I	Hi-z	Negative Voltage Reference Input Pin, VSS2
21	VCOM	O	500 Ω Pull-down	Common Voltage Output Pin, AVDD × 1/2 Large external capacitor 2.2 μF ± 50% is used to reduce power-supply noise.
22	VSS2	-	-	Analog Ground Pin
23	AVDD	-	-	Analog Power Supply Pin, 3.0 V to 3.6 V
24	AOUTL3	O	Hi-z	Lch Analog Output Pin
25	AOUTR3	O	Hi-z	Rch Analog Output Pin
26	AOUTL4	O	Hi-z	Lch Analog Output Pin
27	AOUTR4	O	Hi-z	Rch Analog Output Pin
28	TEST	I	25 kΩ Pull-down	Test Pin. This pin must be connected to VSS1.
29	I2C	I	Hi-z	Control Mode Select Pin "L": 3-wire Serial Control mode "H": I²C Bus Control mode or Parallel Control mode.
30	TVDD	-	-	Digital Power Supply Pin, 1.7 V to 3.6 V
31	VSS1	-	-	Digital Ground Pin
32	LDOO	O	580 Ω Pull-down	LDO Output Pin. This pin must be connected to ground with 2.2 μF ± 50%.

Note 1. All digital input pins must not be allowed to float.

5.3. Handling of Unused Pin

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	AOUTL1–4, AOUTR1–4	Open
Digital	DZF	Open
	SDTI1–4	Connect to VSS1

6. Absolute Maximum Ratings

(VSS1 = VSS2 = 0 V; Note 2)

Parameter	Symbol	Min.	Max.	Unit
Power Supplies				
Analog	AVDD	−0.3	4.3	V
Digital	TVDD	−0.3	4.3	V
Difference (VSS1–2)	ΔGND	−0.3	0.3	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Digital Input Voltage	VIND	−0.3	TVDD + 0.3	V
Ambient Temperature (power applied)	Ta	−40	105	°C
Storage Temperature	Tstg	−65	150	°C

Note 2. All voltages with respect to ground. VSS1 and VSS2 must be connected to the same analog ground plane.

Note 3. The maximum Digital input voltage is smaller value between (LVDD+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1 = VSS2 = 0 V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Analog	AVDD	3.0	3.3	3.6	V
	Digital	TVDD	1.7	3.3	3.6	V
Voltage Reference (Note 5)	“H” voltage reference	VREFH	AVDD − 0.5	-	AVDD	V
	“L” voltage reference	VREFL	-	VSS2	-	V

Note 4. The power up sequence between AVDD and TVDD is not critical.

Note 5. The VREFL pin must be connected to VSS2.

Note 6. Do not turn off the power supply of the AK4438 with the power supply of the peripheral device turned on. When using the I^2C interface, pull-up resistors of SDA and SCL pins should be connected to TVDD or less voltage.

AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Electrical Characteristics

(Ta = 25 °C; AVDD = TVDD = 3.3 V; VSS1 = VSS2 = 0 V; VREFH = AVDD; fs = 48 kHz; BICK = 64fs; Signal Frequency = 1 kHz; 32-bit Data; Measurement Frequency = 20 Hz to 20 kHz at 48 kHz, 20Hz to 40 kHz at fs = 96 kHz, 20 Hz to 40 kHz at fs = 192 kHz, unless otherwise specified.)

Parameter		Min.	Typ.	Max.	Unit
DAC Analog Output Characteristics					
Resolution		-	-	32	bit
Output Voltage (Note 7)		2.55	2.83	3.11	Vpp
S/(N+D) (0 dBFS)	fs = 48 kHz	80	91	-	dB
	fs = 96 kHz	-	89	-	dB
	fs = 192 kHz	-	89	-	dB
Dynamic Range (−60 dBFS)	fs = 48 kHz (A-weighted)	104	108	-	dB
	fs = 96 kHz	-	101	-	dB
	fs = 192 kHz	-	101	-	dB
S/N	fs = 48 kHz (A-weighted)	104	108	-	dB
	fs = 96 kHz	-	101	-	dB
	fs = 192 kHz	-	101	-	dB
Interchannel Isolation		90	110	-	dB
Interchannel Gain Mismatch		-	0	0.7	dB
Load Resistance (Note 8)		10	-	-	kΩ
Load Capacitance		-	-	30	pF
Power Supply Rejection (Note 9)		-	50	-	dB

Note 7. Full-scale output voltage. The output voltage is always proportional to AVDD (AVDD × 0.86).
Note 8. AC Load
Note 9. This is a value when applying a 1kHz 50mVpp sine wave to AVDD.

Parameter	Min.	Typ.	Max.	Unit
Power Supplies				
Power Supply Current				
Normal Operation (PDN pin = “H”)				
AVDD fs = 48 kHz, 96 kHz, 192 kHz	-	27	36	mA
TVDD fs = 48 kHz	-	3.4	4.5	mA
TVDD fs = 96 kHz	-	4.9	6.4	mA
TVDD fs = 192 kHz	-	8.0	10.4	mA
Power-down mode (PDN pin = “L”) (Note 10)				
AVDD + TVDD		10	200	μA

Note 10. Quiescent Current. All digital input pins including clock pins are fixed to VSS.

9. Filter Characteristics

(Ta = −40 °C to +105 °C; AVDD = 3.0 V to 3.6 V, TVDD = 1.7 V to 3.6 V; De-emphasis = OFF)

9.1. Sharp Roll-Off Filter (SD bit = "0", SLOW bit = "0")

fs = 44.1 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 11)	±0.05 dB	PB	0	-	20.0	kHz
	−3.0 dB	PB	-	21.5	-	kHz
Passband Ripple (Note 12)		PR	−0.0032	-	0.0032	dB
Stopband (Note 11)		SB	24.1	-	-	kHz
Stopband Attenuation (Note 14)		SA	80	-	-	dB
Group Delay (Note 13)		GD	-	26.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response: 0 to 20.0 kHz			−0.26	-	0.1	dB

fs = 96 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 11)	±0.05 dB	PB	0	-	43.5	kHz
	−3.0 dB	PB	-	46.8	-	kHz
Passband Ripple (Note 12)		PR	−0.0032	-	0.0032	dB
Stopband (Note 11)		SB	52.5	-	-	kHz
Stopband Attenuation (Note 14)		SA	80	-	-	dB
Group Delay (Note 13)		GD	-	26.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 to 40.0 kHz			−0.53	-	0.1	dB

fs = 192 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 11)	±0.05 dB	PB	0	-	87.0	kHz
	−3.0 dB	PB	-	93.6	-	kHz
Passband Ripple (Note 12)		PR	−0.0032	-	0.0032	dB
Stopband (Note 11)		SB	105	-	-	kHz
Stopband Attenuation (Note 14)		SA	80	-	-	dB
Group Delay (Note 13)		GD	-	26.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 to 80.0kHz			−1.9	-	0.1	dB

Note 11. The pass band and stop band frequencies scale with fs. For example, PB = 0.4535 × fs, SB = 0.546 × fs

Note 12. It is the pass band gain amplitude of the double over sampling filter at the first step of the Interpolator.

Note 13. This delay is the time from setting the 16/20/24/32-bit data of both channels to input register to the output of analog signal.

Note 14. The output level is assumed as 0 dB when inputting a 1 kHz, 0 dB sine wave data.

∗ Digital filter characteristics are based on simulation results.

9.2. Slow Roll-Off Filter (SD bit = "0", SLOW bit = "1")

fs = 44.1 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 15)	±0.05 dB	PB	0	-	8.1	kHz
	−3.0 dB	PB	-	18.2	-	kHz
Passband Ripple (Note 12)		PR	−0.043	-	0.0032	dB
Stopband (Note 15)		SB	39.2	-	-	kHz
Stopband Attenuation (Note 14)		SA	73	-	-	dB
Group Delay (Note 13)		GD	-	6.3	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response: 0 to 20.0 kHz			−5.06	-	0.1	dB

fs = 96 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 15)	±0.05 dB	PB	0	-	17.7	kHz
	−3.0 dB	PB	-	39.5	-	kHz
Passband Ripple (Note 12)		PR	−0.043	-	0.043	dB
Stopband (Note 15)		SB	85.3	-	-	kHz
Stopband Attenuation (Note 14)		SA	73	-	-	dB
Group Delay (Note 13)		GD	-	6.3	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response: 0 to 40.0 kHz			−5.23	-	0.1	dB

fs = 192 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 15)	±0.05 dB	PB	0	-	35.5	kHz
	−3.0 dB	PB	-	79.0	-	kHz
Passband Ripple (Note 12)		PR	−0.043	-	0.043	dB
Stopband (Note 15)		SB	171	-	-	kHz
Stopband Attenuation (Note 14)		SA	73	-	-	dB
Group Delay (Note 13)		GD	-	6.3	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response: 0 to 80.0 kHz			−5.90	-	0.1	dB

Note 15. The pass band and stop band frequencies scale with fs. For example, PB = 0.185 × fs, SB = 0.888 × fs.

9.3. Short Delay Sharp Roll-Off Filter (SD bit = "1", SLOW bit = "0")

fs = 44.1 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 11)	±0.05 dB	PB	0	-	20.0	kHz
	−3.0 dB	PB	-	21.5	-	kHz
Passband Ripple (Note 12)		PR	−0.0031	-	0.0031	dB
Stopband (Note 11)		SB	24.1	-	-	kHz
Stopband Attenuation (Note 14)		SA	80	-	-	dB
Group Delay (Note 13)		GD	-	5.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 to 20.0 kHz			−0.26	-	0.1	dB

fs = 96 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 11)	±0.05 dB	PB	0	-	43.5	kHz
	−3.0 dB	PB	-	46.8	-	kHz
Passband Ripple (Note 12)		PR	-0.0031	-	0.0031	dB
Stopband (Note 11)		SB	52.5	-	-	kHz
Stopband Attenuation (Note 14)		SA	80	-	-	dB
Group Delay (Note 13)		GD	-	5.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 to 40.0 kHz			−0.53	-	0.1	dB

fs = 192 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 11)	±0.05 dB	PB	0	-	87.0	kHz
	−3.0 dB	PB	-	93.6	-	kHz
Passband Ripple (Note 12)		PR	−0.0031	-	0.0031	dB
Stopband (Note 11)		SB	105	-	-	kHz
Stopband Attenuation (Note 14)		SA	80	-	-	dB
Group Delay (Note 13)		GD	-	5.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 to 80.0 kHz			−1.9	-	0.1	dB

9.4. Short Delay Slow Roll-Off Filter (SD bit = "1", SLOW bit = "1")

fs = 44.1 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 16)	±0.05 dB	PB	0	-	11.1	kHz
	−3.0 dB	PB	-	19.4	-	kHz
Passband Ripple	(Note 12)	PR	−0.05	-	0.05	dB
Stopband	(Note 16)	SB	38.1	-	-	kHz
Stopband Attenuation	(Note 14)	SA	82	-	-	dB
Group Delay	(Note 13)	GD	-	4.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 to 20.0kHz			−5.06	-	0.1	dB

fs = 96 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 16)	±0.05 dB	PB	0	-	24.2	kHz
	−3.0 dB	PB	-	42.1	-	kHz
Passband Ripple	(Note 12)	PR	−0.05	-	0.05	dB
Stopband	(Note 16)	SB	83.0	-	-	kHz
Stopband Attenuation	(Note 14)	SA	82	-	-	dB
Group Delay	(Note 13)	GD	-	4.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 to 40.0kHz			−5.23	-	0.1	dB

fs = 192 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 16)	±0.05 dB	PB	0	-	48.4	kHz
	−3.0 dB	PB	-	84.3	-	kHz
Passband Ripple	(Note 12)	PR	−0.05	-	0.05	dB
Stopband	(Note 16)	SB	165.9	-	-	kHz
Stopband Attenuation	(Note 14)	SA	82	-	-	dB
Group Delay	(Note 13)	GD	-	4.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 to 80.0kHz			−5.90	-	0.1	dB

Note 16. The pass band and stop band frequencies scale with fs. For example, PB = 0.252 × fs, SB = 0.864 × fs.

10. DC Characteristics

(Ta = −40 °C to +105°C; AVDD = 3.0 V to 3.6V, TVDD = 1.7 V to 3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
TVDD = 1.7 V to 3.0 V					
High-Level Input Voltage	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	20%TVDD	V
TVDD = 3.0 V to 3.6 V					
High-Level Input Voltage	VIH	70%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%TVDD	V
High-Level Output Voltage					
(DZF pin: Iout = −100 μA)	VOH1	TVDD−0.5	-	-	V
Low-Level Output Voltage					
(DZF pin: Iout= 100 μA)	VOL1	-	-	0.5	V
(SDA pin, 2.0 V ≤ TVDD ≤ 3.6 V: Iout = 3 mA)	VOL2	-	-	0.4	V
(SDA pin, 1.7 V ≤ TVDD ≤ 2.0 V: Iout = 3 mA)	VOL2	-		20%TVDD	V
Input Leakage Current	Iin	-	-	±10	μA

11. Switching Characteristics

(Ta = −40 °C to 105°C; AVDD = 3.0 V to 3.6 V, TVDD = 1.7 V to 3.6 V; C_L = 20 pF, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock (MCLK) Timing					
256fsn:					
Frequency	fCLK	2.048	-	12.288	MHz
Pulse Width Low	tCLKL	32	-	-	ns
Pulse Width High	tCLKH	32	-	-	ns
384fsn:					
Frequency	fCLK	3.072	-	18.432	MHz
Pulse Width Low	tCLKL	22	-	-	ns
Pulse Width High	tCLKH	22	-	-	ns
512fsn, 256fsd, 128fsq, 64fso, 32fsh:					
Frequency	fCLK	4.096	-	24.576	MHz
Pulse Width Low	tCLKL	16	-	-	ns
Pulse Width High	tCLKH	16	-	-	ns
768fsn, 384fsd, 192fsq, 96fso, 48fsh:					
Frequency	fCLK	6.144	-	36.864	MHz
Pulse Width Low	tCLKL	11	-	-	ns
Pulse Width High	tCLKH	11	-	-	ns
LRCK Timing					
Normal mode					
(TDM1-0 bits / pins = “00” / ”LL”)					
Frequency (fs) Normal Speed mode	fsn	8	-	48	kHz
Double Speed mode	fsd	48	-	96	kHz
Quad Speed mode	fsq	96	-	192	kHz
Oct Speed mode	fso	-	384	-	kHz
Hex Speed mode	fsh	-	768	-	kHz
Duty Cycle	Duty	45	-	55	%
TDM128 mode					
(TDM1-0 bits / pins = “01” / ”LH”)	fsn				
Frequency (fs) Normal Speed mode	fsd	8	-	48	kHz
Double Speed mode	fsq	48	-	96	kHz
Quad Speed mode	tLRH	96	-	192	kHz
“H” time	tLRL	1/128fs	-	-	ns
“L” time		1/128fs	-	-	ns
TDM256 mode					
(TDM1-0 bits / pins = “10” / ”HL”)	fsn				
Frequency (fs) Normal Speed mode	fsd	8	-	48	kHz
Double Speed mode	tLRH	48	-	96	kHz
“H” time	tLRL	1/256fs	-	-	ns
“L” time		1/256fs	-	-	ns
TDM512 mode					
(TDM1-0 bits / pins = “11” / ”HH”)	fsn				
Frequency (fs) Normal Speed mode	tLRH	8	-	48	kHz
“H” time	tLRL	1/512fs	-	-	ns
“L” time		1/512fs	-	-	ns

Parameter			Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing							
Normal mode							
(TDM1-0 bits / pins = “00” / ”LL”)							
BICK Period	Normal Speed Mode		tBCK	1/256fsn	-	-	ns
	Double Speed Mode		tBCK	1/128fsd	-	-	ns
	Quad Speed Mode		tBCK	1/64fsq	-	-	ns
	Oct Speed Mode		tBCK	1/64fso	-	-	ns
	Hex Speed Mode		tBCK	1/64fsh	-	-	ns
BICK Pulse Width Low			tBCKL	9	-	-	ns
BICK Pulse Width High			tBCKH	9	-	-	ns
LRCK Edge to BICK “↑”		(Note 17)	tLRB	5	-	-	ns
BICK “↑” to LRCK Edge		(Note 17)	tBLR	5	-	-	ns
SDTI Hold Time			tSDH	5	-	-	ns
SDTI Setup Time			tSDS	5	-	-	ns
TDM128 mode							
(TDM1-0 bits / pins = “01” / ”LH”)							
BICK Period	Normal Speed Mode		tBCK	1/128fsn	-	-	ns
	Double Speed Mode		tBCK	1/128fsd	-	-	ns
	Quad Speed Mode		tBCK	1/128fsq	-	-	ns
BICK Pulse Width Low			tBCKL	16	-	-	ns
BICK Pulse Width High			tBCKH	16	-	-	ns
LRCK Edge to BICK “↑”		(Note 17)	tLRB	5	-	-	ns
BICK “↑” to LRCK Edge		(Note 17)	tBLR	5	-	-	ns
SDTI Hold Time			tSDH	5	-	-	ns
SDTI Setup Time			tSDS	5	-	-	ns
TDM256 mode							
(TDM1-0 bits / pins = “10” / ”HL”)							
BICK Period	Normal Speed Mode		tBCK	1/256fsn	-	-	ns
	Double Speed Mode		tBCK	1/256fsd	-	-	ns
BICK Pulse Width Low			tBCKL	16	-	-	ns
BICK Pulse Width High			tBCKH	16	-	-	ns
LRCK Edge to BICK “↑”		(Note 17)	tLRB	5	-	-	ns
BICK “↑” to LRCK Edge		(Note 17)	tBLR	5	-	-	ns
SDTI Hold Time			tSDH	5	-	-	ns
SDTI Setup Time			tSDS	5	-	-	ns
TDM512 mode							
(TDM1-0 bits / pins = “11” / ”HH”)							
BICK Period	Normal Speed Mode		tBCK	1/512fsn	-	-	ns
BICK Pulse Width Low			tBCKL	16	-	-	ns
BICK Pulse Width High			tBCKH	16	-	-	ns
LRCK Edge to BICK “↑”		(Note 17)	tLRB	5	-	-	ns
BICK “↑” to LRCK Edge		(Note 17)	tBLR	5	-	-	ns
SDTI Hold Time			tSDH	5	-	-	ns
SDTI Setup Time			tSDS	5	-	-	ns

Note 17. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (3-wire Serial Control mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
Control Interface Timing (I^2C Bus Control mode)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 18)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 19)	tAPD	800	-	-	ns
PDN Reject Pulse Width	tRPD	-	-	50	ns

Note 18. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 19. The AK4438 can be reset by setting the PDN pin to "L" upon power-up. The PDN pin must held "L" for more than 800ns for a certain reset. The AK4438 is not reset by the "L" pulse less than 50ns.

Note 20. I^2C-bus is a trademark of NXP B.V.

11.1. Timing Diagram

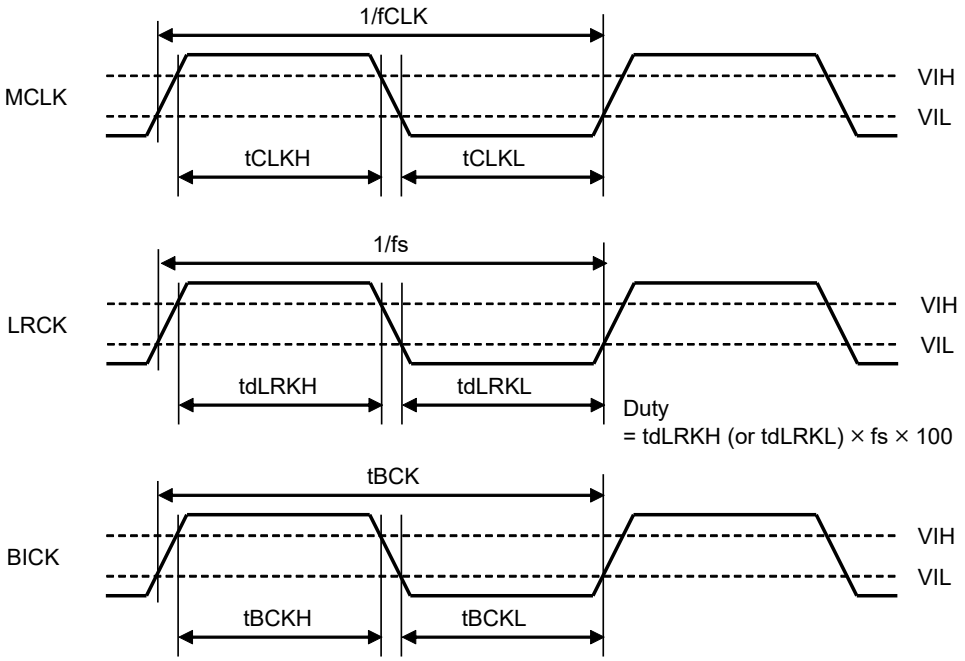


Figure 3. Clock Timing (TDM1-0 bits = “00”)

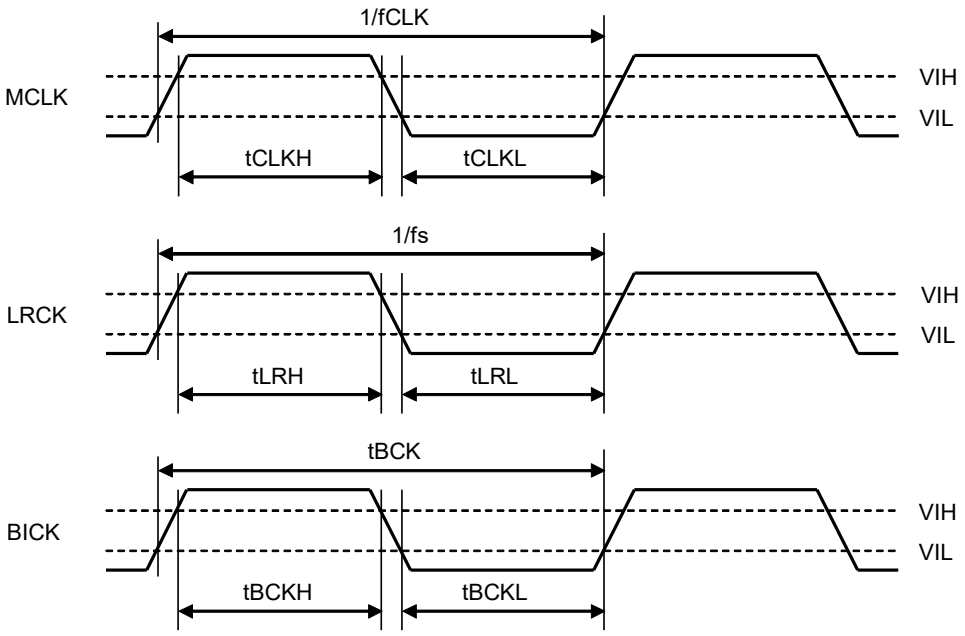


Figure 4. Clock Timing (Except TDM1-0 bits = “00”)

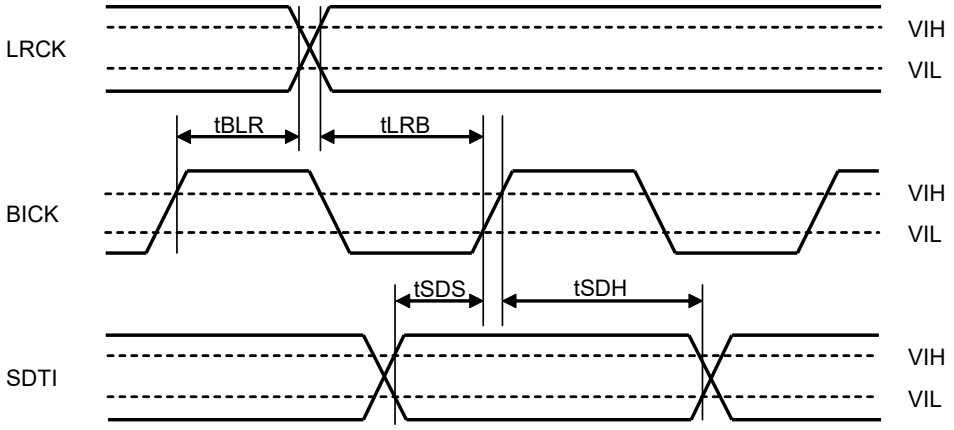


Figure 5. Audio Interface Timing

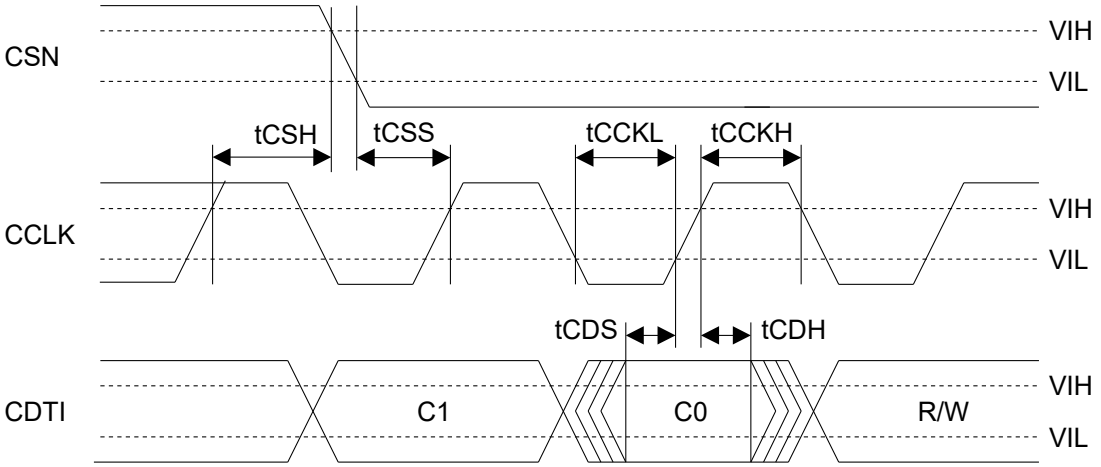


Figure 6. WRITE Command Input Timing (3-wire Serial Control mode)

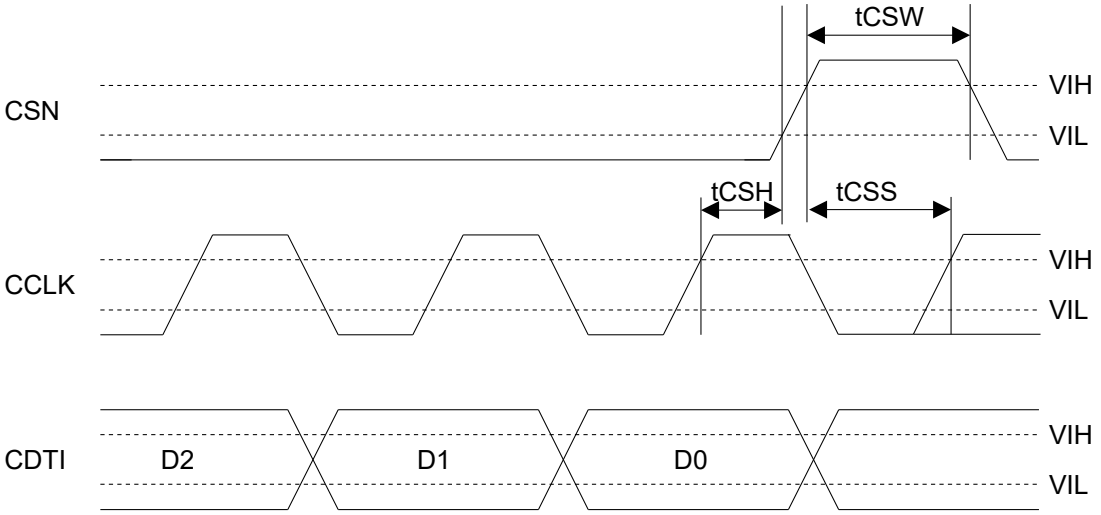


Figure 7. WRITE Data Input Timing (3-wire Serial Control mode)

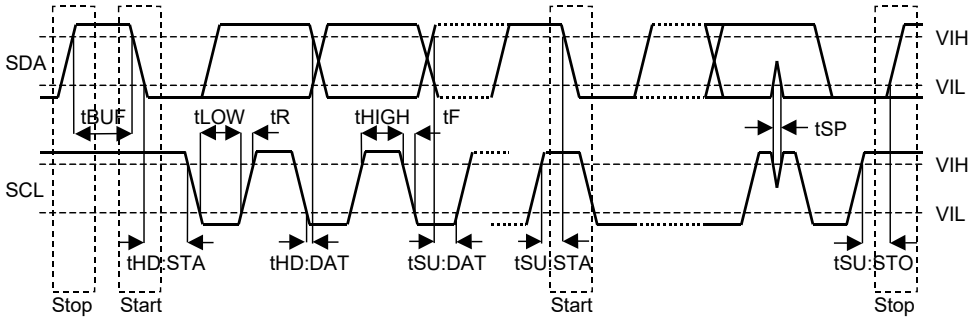


Figure 8. I²C Bus Control mode Timing

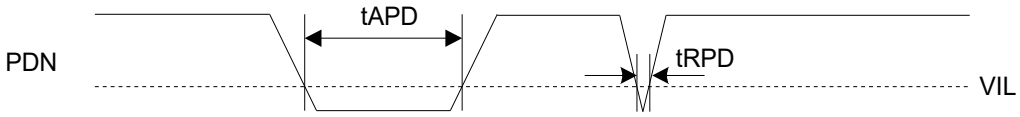


Figure 9. Power-down & Reset Timing

12. Function Descriptions

12.1. System Clock

The external clocks which are required to operate the AK4438 are MCLK, LRCK and BICK. MCLK should be synchronized with LRCK and BICK, but the phase is not critical. There are two ways to set the clocks: Manual Setting mode and Auto Setting mode, which are selected by the ACKS bit. When ACKS bit = “0”, it is in Manual Setting mode, and when ACKS bit = “1”, it is in Auto Setting mode. In Parallel Control mode, it is in Auto Setting mode.

When changing the clock, the AK4438 must be reset by the PDN pin or RSTN bit.

If the clock is stopped, a click noise occurs when restarting the clock. Mute the analog output externally if the click noise affects system applications.

12.1.1. Manual Setting mode (ACKS bit = “0”)

Set the sampling speed mode by DFS2–0 bits (Table 1). Input MCLK with the frequency shown in Table 2 and Table 3 according to the sampling speed mode. When DFS2–0 bits are changed, the AK4438 should be reset by RSTN bit.

DFS2	DFS1	DFS0	Sampling Speed Mode (fs)		
0	0	0	Normal Speed mode	8 kHz – 48 kHz	(default)
0	0	1	Double Speed mode	48 kHz – 96 kHz	
0	1	0	Quad Speed mode	96 kHz – 192 kHz	
0	1	1	N/A	N/A	
1	0	0	Oct Speed mode	384 kHz	
1	0	1	Hex Speed mode	768 kHz	
1	1	0	N/A	N/A	
1	1	1	N/A	N/A	

(N/A: Not Available)

Table 1. Sampling Speed Mode (Manual Setting mode)

LRCK	MCLK Frequency [MHz]				Sampling Speed Mode
fs	32fs	48fs	64fs	96fs	
8.0 kHz	N/A	N/A	N/A	N/A	Normal
44.1 kHz	N/A	N/A	N/A	N/A	
48.0 kHz	N/A	N/A	N/A	N/A	
88.2 kHz	N/A	N/A	N/A	N/A	Double
96.0 kHz	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	Quad
192.0 kHz	N/A	N/A	N/A	N/A	
384.0 kHz	N/A	N/A	24.576	36.864	Oct
768.0 kHz	24.576	36.864	N/A	N/A	Hex

Table 2. Combination of Sampling Frequency and MCLK Frequency (Manual Setting mode)

LRCK	MCLK Frequency [MHz]						Sampling Speed Mode
fs	128fs	192fs	256fs	384fs	512fs	768fs	
8.0 kHz	N/A	N/A	2.0480	3.0720	4.0960	6.1440	Normal
44.1 kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	
48.0 kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	
88.2 kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	Double
96.0 kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	
176.4 kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	Quad
192.0 kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	
384.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Hex

Table 3. Combination of Sampling Frequency and MCLK Frequency (Manual Setting mode)

12.1.2. Auto Setting mode (ACKS bit = “1”)

The Sampling Speed Mode is detected automatically, and DFS2-0 bits are ignored (Table 4). Supply MCLK with the frequency shown in Table 5 and Table 6 according to the Sampling Speed Mode.

MCLK		Sampling Speed Mode
512fs/256fs	768fs/384fs	Normal Speed mode
256fs	384fs	Double Speed mode
128fs	192fs	Quad Speed mode
64fs	96fs	Oct Speed mode
32fs	48fs	Hex Speed mode

Table 4. Sampling Speed Mode and Available MCLK Frequency (Auto Setting mode)

LRCK	MCLK Frequency [MHz]				Sampling Speed Mode
fs	32fs	48fs	64fs	96fs	
8.0 kHz	N/A	N/A	N/A	N/A	Normal
44.1 kHz	N/A	N/A	N/A	N/A	
48.0 kHz	N/A	N/A	N/A	N/A	
88.2 kHz	N/A	N/A	N/A	N/A	Double
96.0 kHz	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	Quad
192.0 kHz	N/A	N/A	N/A	N/A	
384.0 kHz	N/A	N/A	24.576	36.864	Oct
768.0 kHz	24.576	36.864	N/A	N/A	Hex

Table 5. Combination of Sampling Frequency and MCLK Frequency (Auto Setting mode)

LRCK	MCLK Frequency [MHz]						Sampling Speed Mode
fs	128fs	192fs	256fs	384fs	512fs	768fs	
8.0 kHz	N/A	N/A	2.0480	3.0720	4.0960	6.1440	Normal
44.1 kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	
48.0 kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	
88.2 kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	Double
96.0 kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	
176.4 kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	Quad
192.0 kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	
384.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Hex

Table 6. Combination of Sampling Frequency and MCLK Frequency (Auto Setting mode)

In Auto Setting mode, like Manual Setting mode, MCLK of 256fs or 384fs can be used for sampling frequencies from 8 kHz to 48 kHz, but the dynamic range and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs. (Table 7)

MCLK Freq.	Dynamic Range, S/N	
	Manual Setting mode	Auto Setting mode
256fs, 384fs	108 dB	105 dB
512fs, 768fs	108 dB	108 dB

Table 7. Relationship of DR, S/N and MCLK frequency when fs = 44.1kHz

12.2. De-emphasis Filter

The AK4438 has a digital de-emphasis filter (tc=50/15μs) by an IIR filter. DEMx1–0 bits (x = 1–4) select the assumed sampling frequency of the de-emphasis filter for each DAC. The de-emphasis filter is only available in Normal Speed mode. In other sampling speed modes, the de-emphasis filter is turned off regardless of DEMx1-0 bits setting.

DEMx1 bit	DEMx0 bit	Sampling Frequency	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 8. De-emphasis Filter Control

12.3. Audio Interface Format

The audio data is shifted in via the SDTI1–4 pins using BICK and LRCK inputs. The audio data is MSB first, 2's compliment and is latched on the rising edge of BICK. The audio interface format is selected by the TDM1–0 bits and DIF2–0 bits (Table 9). If the bit length of the input audio data is shorter than the bit length of the data format listed in the table, fill the lower bits with "0". In parallel control mode, the audio interface format can be selected by the TDM1–0 pins and the DIF pin, but the available formats are limited. (Table 22)
TDM1–0 bits, DIF2–0 bits, TDM1-0 pins, DIF pin settings should not be changed during operation.

Normal Mode (TDM1–0 bits = "00" or TDM1–0 pins = "LL")
Two channel data are input from each of the SDTI1–4 pins, for a total of eight channels of data. There are eight different data formats.

TDM128 Mode (TDM1–0 bits = "01" or TDM1–0 pins = "LH")
Four channel data are input from each of the SDTI1–2 pins, for a total of eight channels of data. The data input to SDTI3-4 pins are ignored. BICK frequency is fixed at 128fs. There are six different data formats.

TDM256 Mode (TDM1–0 bits = "10" or TDM1–0 pins = "HL")
Eight channel data are input from each of the SDTI1–2 pins, for a total of sixteen channels of data. The data input to SDTI3-4 pins are ignored. BICK frequency is fixed at 256fs. There are six different data formats.

TDM512 Mode (TDM1–0 bits = "11" or TDM1–0 pins = "HH")
Sixteen channel data are input from the SDTI1 pin. The data input to SDTI2–4 pins are ignored. BICK frequency is fixed at 512fs. There are six different data formats.

Mode		TDM1 bit	TDM0 bit	DIF2 bit	DIF1 bit	DIF0 bit	Data Format	LRCK	BICK
Normal (Note 21)	0	0	0	0	0	0	16-bit LSB justified	H/L	≥32fs
	1			0	0	1	20-bit LSB justified	H/L	≥40fs
	2			0	1	0	24-bit MSB justified	H/L	≥48fs
	3			0	1	1	16-bit I²S compatible	L/H	32fs
							24-bit I²S compatible	L/H	≥48fs
	4			1	0	0	24-bit LSB justified	H/L	≥48fs
	5			1	0	1	32-bit LSB justified	H/L	≥64fs
	6			1	1	0	32-bit MSB justified	H/L	≥64fs
	7			1	1	1	32-bit I²S compatible	L/H	≥64fs
TDM128	-	0	1	0	0	0	N/A	-	-
	-			0	0	1	N/A	-	-
	8			0	1	0	24-bit MSB justified	↑	128fs
	9			0	1	1	24-bit I²S compatible	↓	128fs
	10			1	0	0	24-bit LSB justified	↑	128fs
	11			1	0	1	32-bit LSB justified	↑	128fs
	12			1	1	0	32-bit MSB justified	↑	128fs
	13			1	1	1	32-bit I²S compatible	↓	128fs
TDM256	-	1	0	0	0	0	N/A	-	-
	-			0	0	1	N/A	-	-
	14			0	1	0	24-bit MSB justified	↑	256fs
	15			0	1	1	24-bit I²S compatible	↓	256fs
	16			1	0	0	24-bit LSB justified	↑	256fs
	17			1	0	1	32-bit LSB justified	↑	256fs
	18			1	1	0	32-bit MSB justified	↑	256fs
	19			1	1	1	32-bit I²S compatible	↓	256fs
TDM512	-	1	1	0	0	0	N/A	-	-
	-			0	0	1	N/A	-	-
	20			0	1	0	24-bit MSB justified	↑	512fs
	21			0	1	1	24-bit I²S compatible	↓	512fs
	22			1	0	0	24-bit LSB justified	↑	512fs
	23			1	0	1	32-bit LSB justified	↑	512fs
	24			1	1	0	32-bit MSB justified	↑	512fs
	25			1	1	1	32-bit I²S compatible	↓	512fs

(N/A: Not Available)

Table 9. Audio Interface Format

Note 21. The number of BICK clocks per channel must be greater than or equal to the bit length of the configuration format, except when set to 16-bit I²S compatible the number of BICK clock periods per channel must be 16.

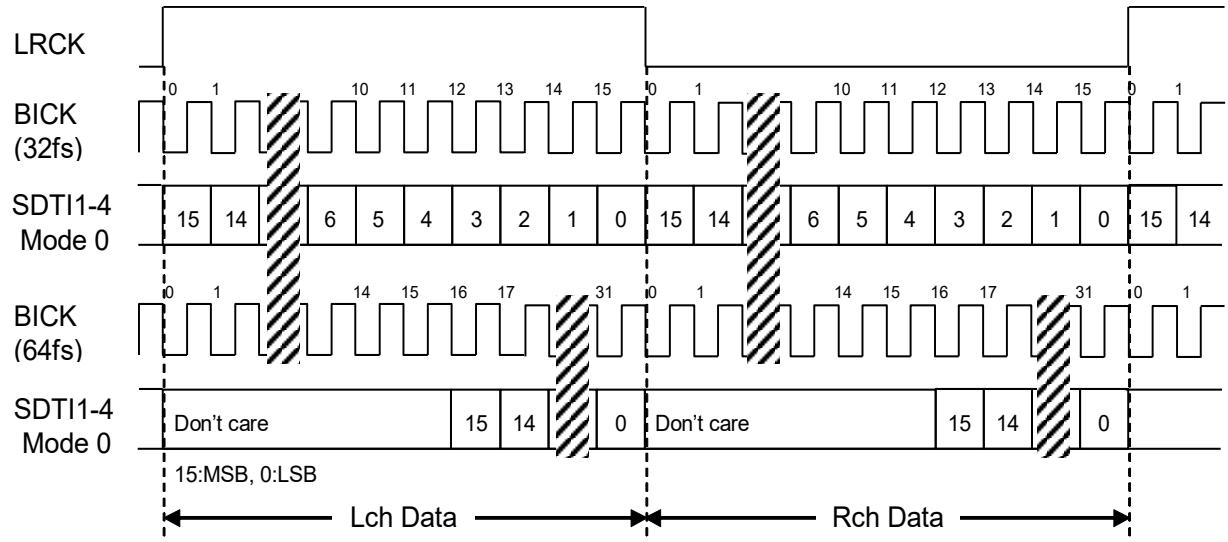


Figure 10. Mode 0 Timing

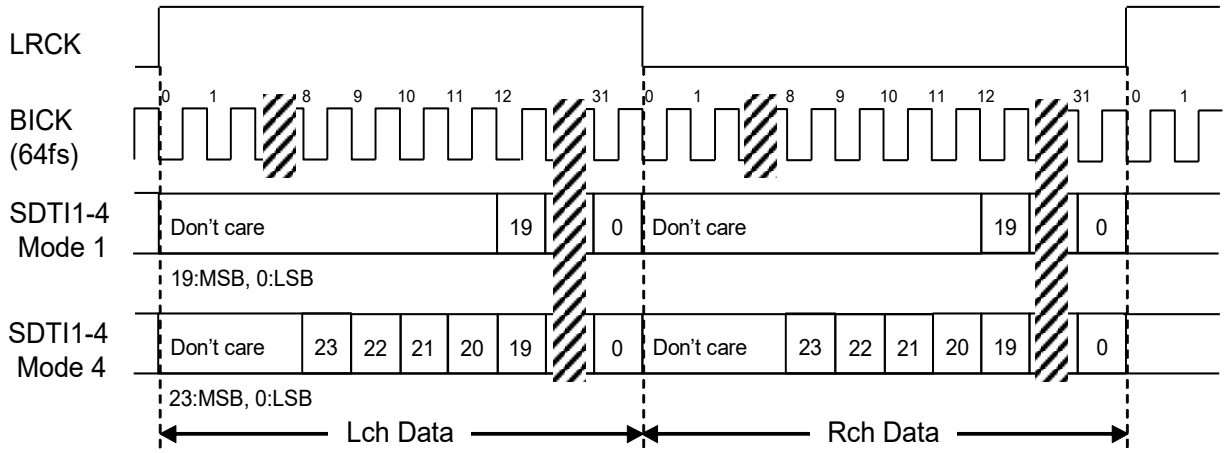


Figure 11. Mode 1/4 Timing

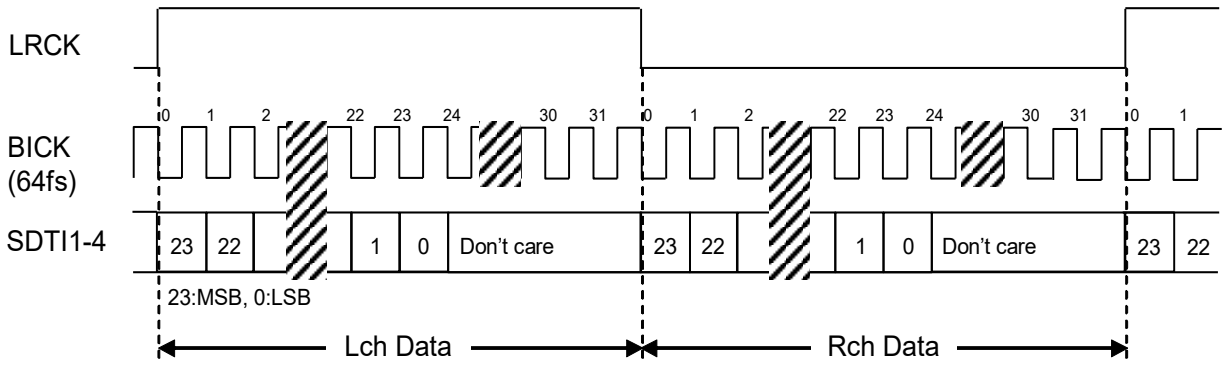


Figure 12. Mode 2 Timing

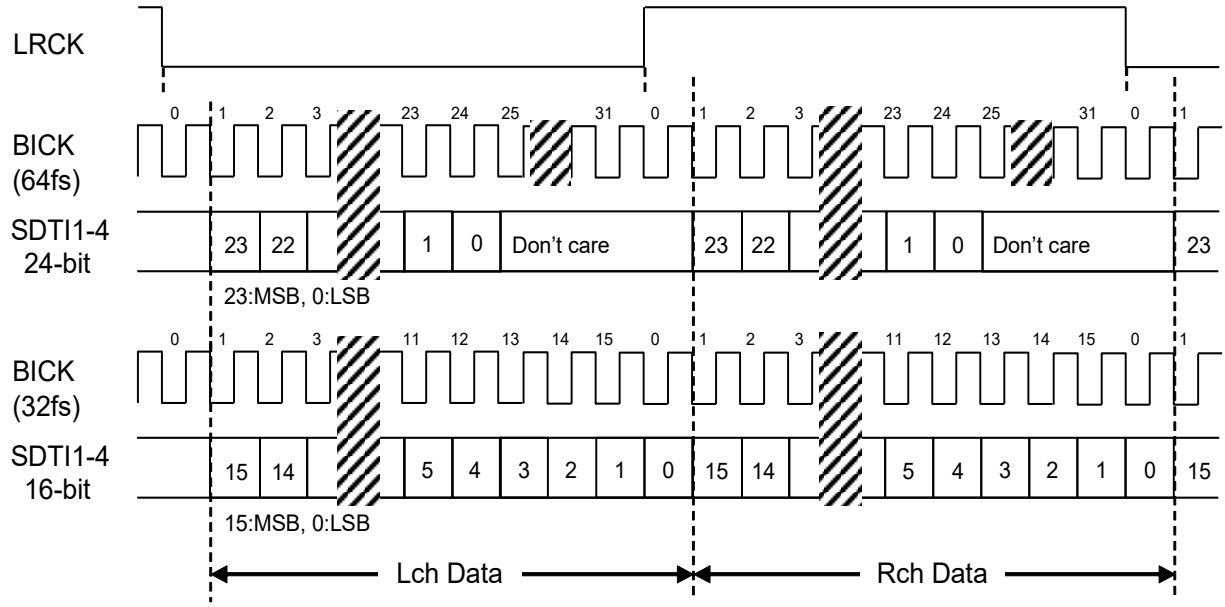


Figure 13. Mode 3 Timing

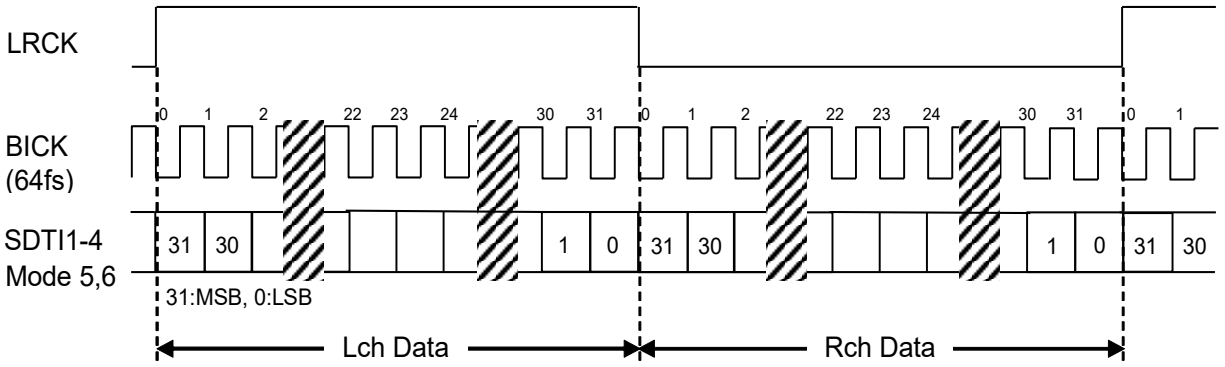


Figure 14. Mode 5/6 Timing

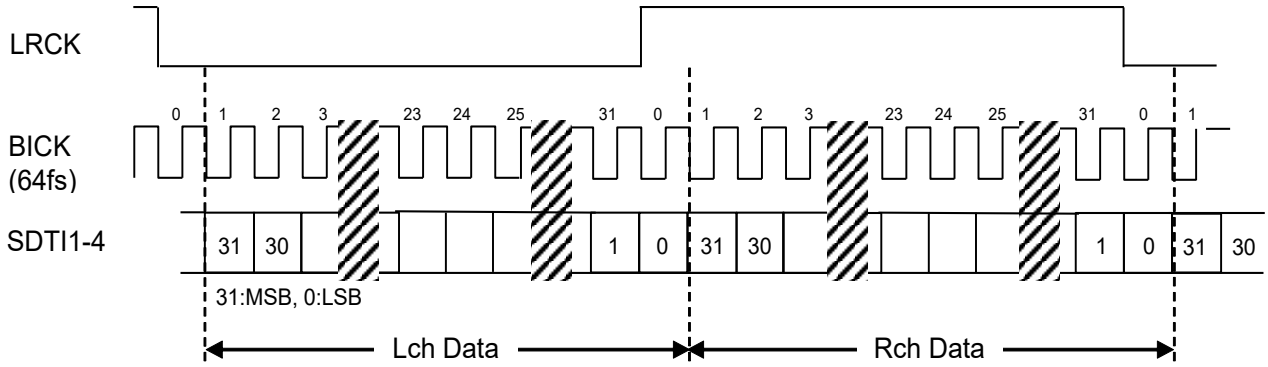


Figure 15. Mode 7 Timing

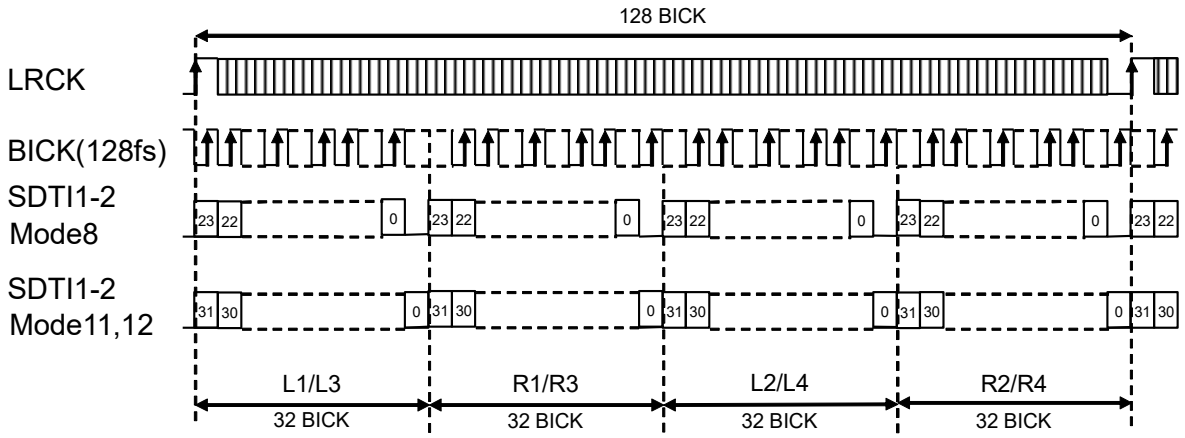


Figure 16. Mode 8/11/12 Timing

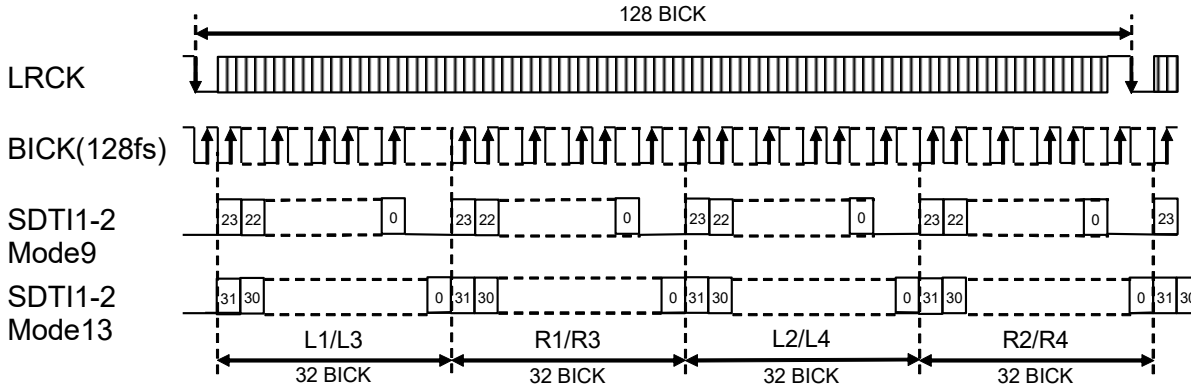


Figure 17. Mode 9/13 Timing

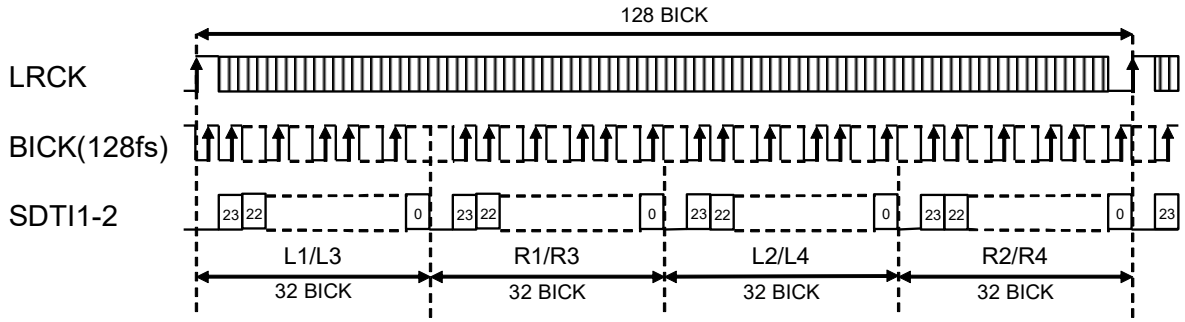


Figure 18. Mode 10 Timing

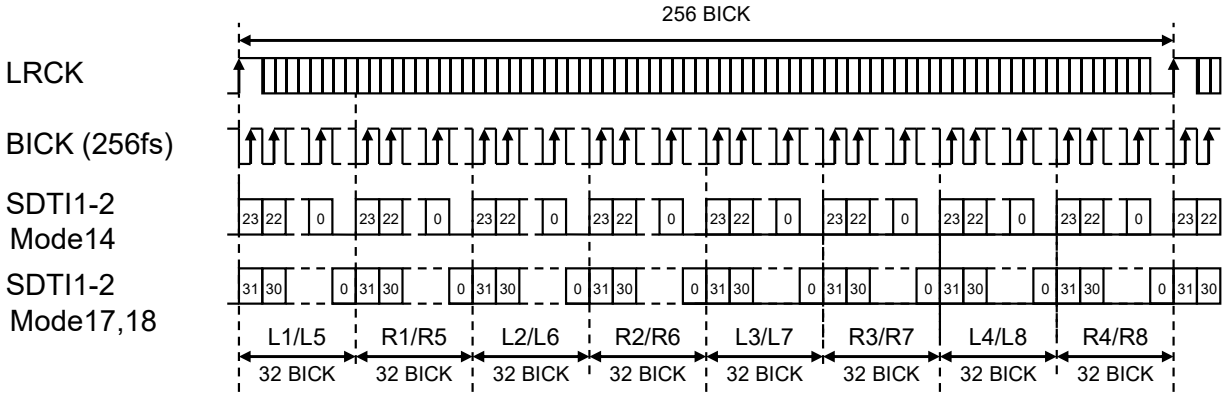


Figure 19. Mode 14/17/18 Timing

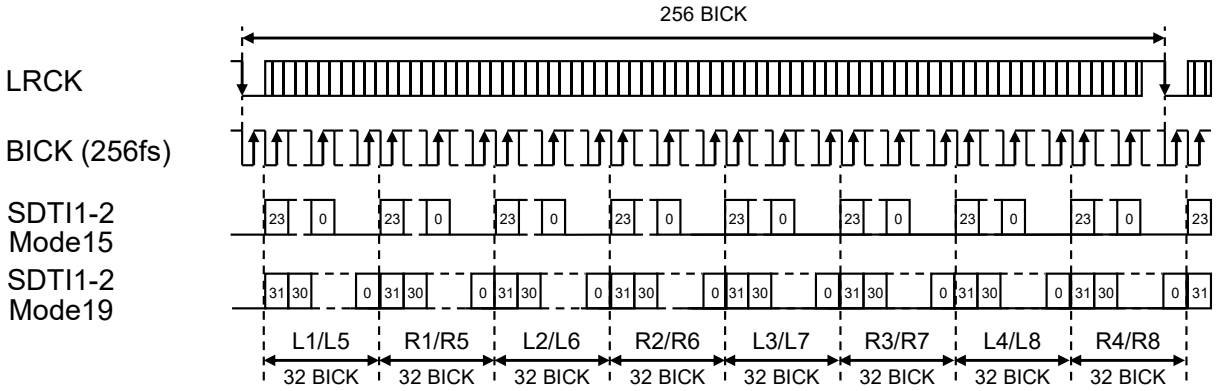


Figure 20. Mode 15/19 Timing

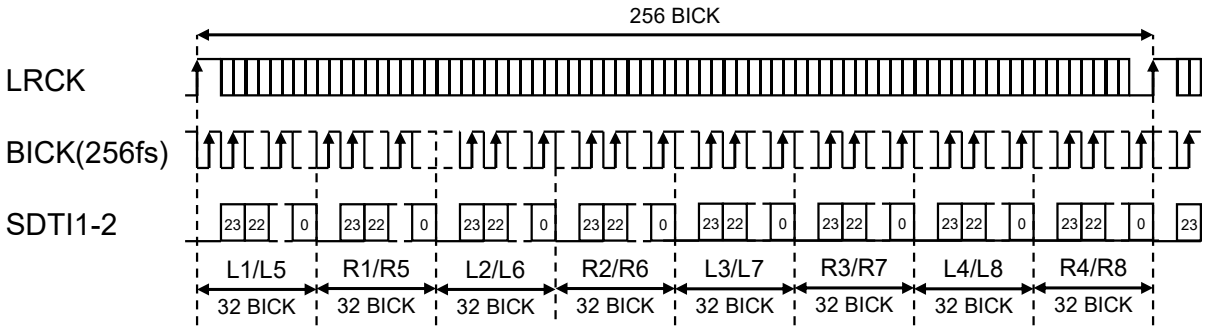


Figure 21. Mode 16 Timing

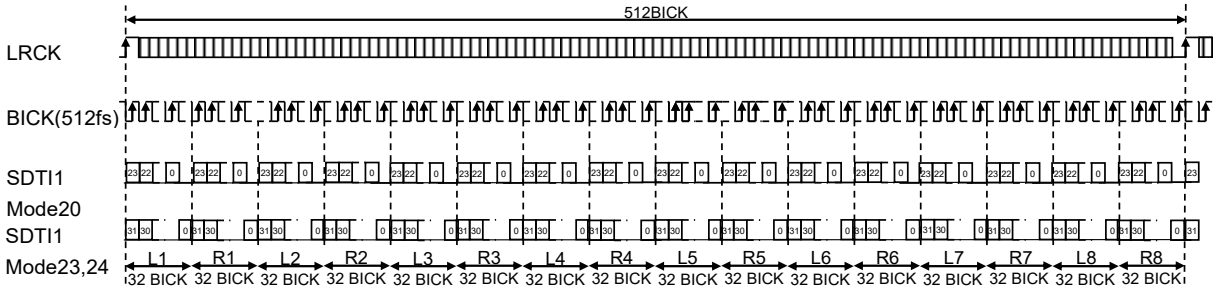


Figure 22. Mode 20/23/24 Timing

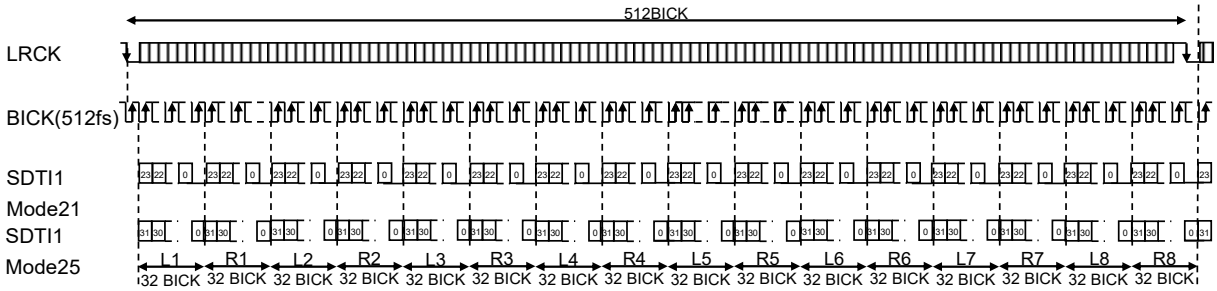


Figure 23. Mode 21/25 Timing

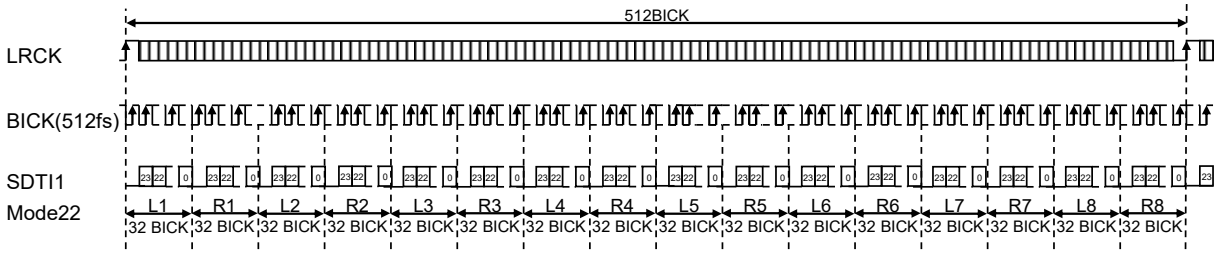


Figure 24. Mode 22 Timing

12.4. Data Select

SDS2–0 bits select the data slot assignment for each DAC. (Table 10) Do not change SDS2–0 bits during operation.

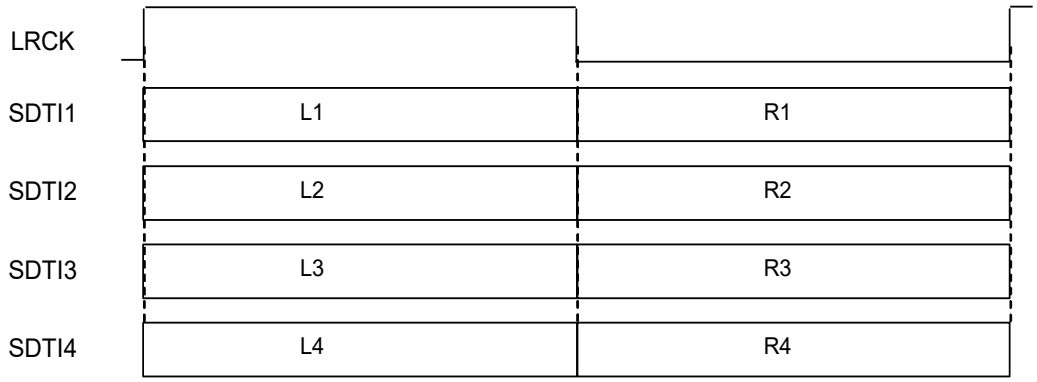


Figure 25. Data Slot in Normal mode

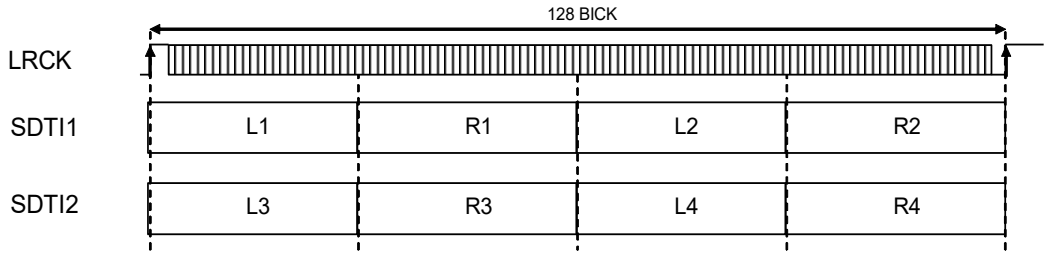


Figure 26. Data Slot in TDM128 mode

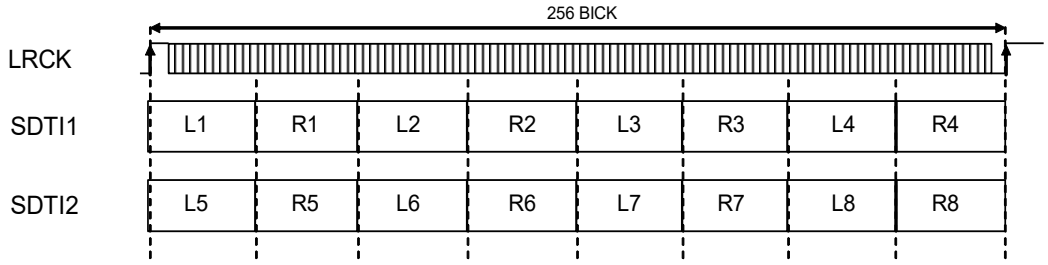


Figure 27. Data Slot in TDM256 mode

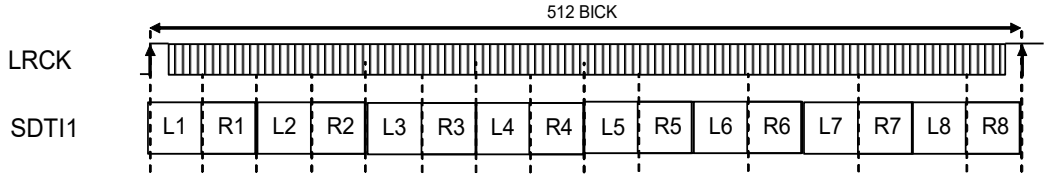


Figure 28. Data Slot in TDM512 mode

Input Mode	SDS2 bit	SDS1 bit	SDS0 bit	Data Slot							
				DAC1		DAC2		DAC3		DAC4	
				Lch	Rch	Lch	Rch	Lch	Rch	Lch	Rch
Normal	*	0	0	L1	R1	L2	R2	L3	R3	L4	R4
	*	0	1	L2	R2	L3	R3	L4	R4	L1	R1
	*	1	0	L3	R3	L4	R4	L1	R1	L2	R2
	*	1	1	L4	R4	L1	R1	L2	R2	L3	R3
TDM128	*	0	0	L1	R1	L2	R2	L3	R3	L4	R4
	*	0	1	L2	R2	L3	R3	L4	R4	L1	R1
	*	1	0	L3	R3	L4	R4	L1	R1	L2	R2
	*	1	1	L4	R4	L1	R1	L2	R2	L3	R3
TDM256	0	0	0	L1	R1	L2	R2	L3	R3	L4	R4
	0	0	1	L2	R2	L3	R3	L4	R4	L5	R5
	0	1	0	L3	R3	L4	R4	L5	R5	L6	R6
	0	1	1	L4	R4	L5	R5	L6	R6	L7	R7
	1	0	0	L5	R5	L6	R6	L7	R7	L8	R8
	1	0	1	L6	R6	L7	R7	L8	R8	L1	R1
	1	1	0	L7	R7	L8	R8	L1	R1	L2	R2
	1	1	1	L8	R8	L1	R1	L2	R2	L3	R3
TDM512	0	0	0	L1	R1	L2	R2	L3	R3	L4	R4
	0	0	1	L2	R2	L3	R3	L4	R4	L5	R5
	0	1	0	L3	R3	L4	R4	L5	R5	L6	R6
	0	1	1	L4	R4	L5	R5	L6	R6	L7	R7
	1	0	0	L5	R5	L6	R6	L7	R7	L8	R8
	1	0	1	L6	R6	L7	R7	L8	R8	L1	R1
	1	1	0	L7	R7	L8	R8	L1	R1	L2	R2
	1	1	1	L8	R8	L1	R1	L2	R2	L3	R3

(*: Do not care)

Table 10. Data Slot Select

12.5. Digital Filter

The filter to be used can be selected from 5 types by setting the SD bit, SLOW bit, and SSLOW bit. Please choose according to purpose and sound preference. The selection is common to DAC1–4.

SSLOW bit	SD bit	SLOW bit	Filter Mode	
0	0	0	Sharp Roll-off Filter	
0	0	1	Slow Roll-off Filter	
0	1	0	Short Delay Sharp Roll-off Filter	(default)
0	1	1	Short Delay Slow Roll-off Filter	
1	*	*	Super Slow Roll-off Filter	

(*:Do not care)

Table 11. Digital Filter Setting

12.6. Zero Detection

AK4438 has a zero-detection function for each channel. The zero-detection circuits monitor the data from the digital volume (DATT)/ soft mute block. When the data is zero for 8192 consecutive LRCK cycles, it is determined to be zero input. The detection result is output to DZF pin. The zero detection for each channel can be enabled by L1-L4, R1-R4 bits. Set to “1” to enable the zero detection. When all channels with enabled detect zero input, the DZF pin goes high. After that, when the data of any channel with zero detection enabled becomes non-zero, the DZF pin goes to “L”. If the RSTN bit is “0”, the DZF pin goes to “H”. The DZF pin go to “L” after 4–5/fs when RSTN bit returns to “1”. If all channels are disabled, the DZF pin outputs “L”. The DZFB bit invert the polarity of the DZF pin.

DZFB bit	DZF pin	
	Not Zero	Zero
0	L	H
1	H	L

Table 12. DZF Pin Polarity

Not Zero: Any of the channels with the detection enabled has a non-zero input..
Zero : All channels with the detection enabled have zero input.

12.7. Digital Volume Function (DATT)

The AK4438 has a channel-independent digital attenuator (256 levels, 0.5dB steps). Attenuation level of each channel is set by ATT7-0 bits. (Table 13).

ATT7–0 bits (Register 03H–04H, 0FH–14H)	Attenuation Level	
FFH	0 dB	(default)
FEH	−0.5 dB	
FDH	−1.0 dB	
:	:	
:	:	
02H	−126.5 dB	
01H	−127.0 dB	
00H	MUTE (−∞ dB)	

Table 13. Attenuation level of Digital Volume

Transition speed of attenuation level can be selected by the ATS1-0 bits (Table 14). The transition of attenuation level is a soft transition in Mode0/1/2 eliminating switching noise in the transition.

Mode	ATS1 bit	ATS0 bit	Attenuation Level Transition Speed (Transition Time form 0 dB to Mute)	
0	0	0	4080/fs	(default)
1	0	1	2040/fs	
2	1	0	510/fs	
3	1	1	255/fs	

Table 14. Transition Time of Digital Volume

In Mode 0, the range from 0 dB to MUTE is divided into 4080 levels. The attenuation level transitions by one level per sampling period. When fs = 48 kHz, it takes 85 ms to go from 0 dB to MUTE.

If the attenuation level setting is changed during reset, the attenuation level will be changed to the setting level after releasing the reset. If the attenuation level setting is changed within 5/fs after releasing a reset, the attenuation level is changed immediately without soft transition. If the PDN pin goes to “L”, ATT7-0 bits are initialized to FFH (0dB).

12.8. LR Channel Output Signal Select

The MONOx and SELLRx bits (x = 1–4) allow the same data to be input to the L and R channels of DACx or the L and R channels to be swapped. The output signal phase of DAC channel is controlled by INVLx and INVRx bits. These functions are available for any audio interface format.

MONO1 bit	SELLR1 bit	INVL1 bit	INVR1 bit	L1ch Out	R1ch Out
0	0	0	0	L1ch In	R1ch In
		1	0	L1ch In Invert	R1ch In
		0	1	L1ch In	R1ch In Invert
		1	1	L1ch In Invert	R1ch In Invert
0	1	0	0	R1ch In	L1ch In
		1	0	R1ch In Invert	L1ch In
		0	1	R1ch In	L1ch In Invert
		1	1	R1ch In Invert	L1ch In Invert
1	0	0	0	L1ch In	L1ch In
		1	0	L1ch In Invert	L1ch In
		0	1	L1ch In	L1ch In Invert
		1	1	L1ch In Invert	L1ch In Invert
1	1	0	0	R1ch In	R1ch In
		1	0	R1ch In Invert	R1ch In
		0	1	R1ch In	R1ch In Invert
		1	1	R1ch In Invert	R1ch In Invert

Table 15. Output Select for DAC1

MONO2 bit	SELLR2 bit	INVL2 bit	INVR2 bit	L2ch Out	R2ch Out
0	0	0	0	L2ch In	R2ch In
		1	0	L2ch In Invert	R2ch In
		0	1	L2ch In	R2ch In Invert
		1	1	L2ch In Invert	R2ch In Invert
0	1	0	0	R2ch In	L2ch In
		1	0	R2ch In Invert	L2ch In
		0	1	R2ch In	L2ch In Invert
		1	1	R2ch In Invert	L2ch In Invert
1	0	0	0	L2ch In	L2ch In
		1	0	L2ch In Invert	L2ch In
		0	1	L2ch In	L2ch In Invert
		1	1	L2ch In Invert	L2ch In Invert
1	1	0	0	R2ch In	R2ch In
		1	0	R2ch In Invert	R2ch In
		0	1	R2ch In	R2ch In Invert
		1	1	R2ch In Invert	R2ch In Invert

Table 16. Output Select for DAC2

MONO3 bit	SELLR3 bit	INVL3 bit	INVR3 bit	L3ch Out	R3ch Out
0	0	0	0	L3ch In	R3ch In
		1	0	L3ch In Invert	R3ch In
		0	1	L3ch In	R3ch In Invert
		1	1	L3ch In Invert	R3ch In Invert
0	1	0	0	R3ch In	L3ch In
		1	0	R3ch In Invert	L3ch In
		0	1	R3ch In	L3ch In Invert
		1	1	R3ch In Invert	L3ch In Invert
1	0	0	0	L3ch In	L3ch In
		1	0	L3ch In Invert	L3ch In
		0	1	L3ch In	L3ch In Invert
		1	1	L3ch In Invert	L3ch In Invert
1	1	0	0	R3ch In	R3ch In
		1	0	R3ch In Invert	R3ch In
		0	1	R3ch In	R3ch In Invert
		1	1	R3ch In Invert	R3ch In Invert

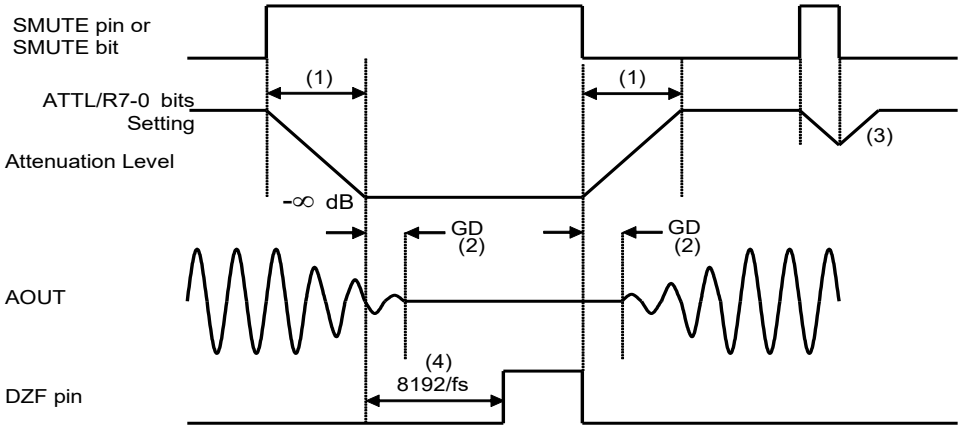
Table 17. Output Select for DAC3

MONO4 bit	SELLR4 bit	INVL4 bit	INVR4 bit	L4	R4
0	0	0	0	L4ch In	R4ch In
		1	0	L4ch In Invert	R4ch In
		0	1	L4ch In	R4ch In Invert
		1	1	L4ch In Invert	R4ch In Invert
0	1	0	0	R4ch In	L4ch In
		1	0	R4ch In Invert	L4ch In
		0	1	R4ch In	L4ch In Invert
		1	1	R4ch In Invert	L4ch In Invert
1	0	0	0	L4ch In	L4ch In
		1	0	L4ch In Invert	L4ch In
		0	1	L4ch In	L4ch In Invert
		1	1	L4ch In Invert	L4ch In Invert
1	1	0	0	R4ch In	R4ch In
		1	0	R4ch In Invert	R4ch In
		0	1	R4ch In	R4ch In Invert
		1	1	R4ch In Invert	R4ch In Invert

Table 18. Output Select for DAC4

12.9. Soft Mute Operation (SMUTE)

The soft mute operation is performed at digital domain. When the SMUTE pin goes “H” or the SMUTE bit is set to '1', the attenuation level will soft transition from the current level to mute (−∞ dB). When the SMUTE pin returns to “L” or the SMUTE bit returns to “0”, the mute is cancelled, and the attenuation level soft transition to the previous level. The transition speed is determined by ATS1–0 bits. If soft mute is cancelled before mute is reached, the transition is discontinued, and the attenuation level returns to the level set by ATTL/R7-0 bits in the same cycle. The soft mute is effective for changing the signal source without stopping the audio data transmission.



Notes:

(1) ATTL/R7–0 bits setting / 255 × Attenuation Level Transition Speed in Table 14
For example, when ATS1–0 bits = “00” and ATTL/R7–0 bits are set to “FFH”, the time required for transition is 4080 LRCK cycles.

(2) The analog output corresponding to the digital input has group delay (GD).

(3) If soft mute is cancelled before mute is reached, the attenuation level returns to the level set by ATTL/R7-0 bits in the same cycle.

(4) When the input data for all zero detection channels are “0” for 8192 consecutive cycles, the DZF pin goes to “H”. After that, when the input data for any channel is not “0”, the DZF pin goes to “L”.

Figure 29. Soft Mute Function and Zero Detection

12.10. Error Detection

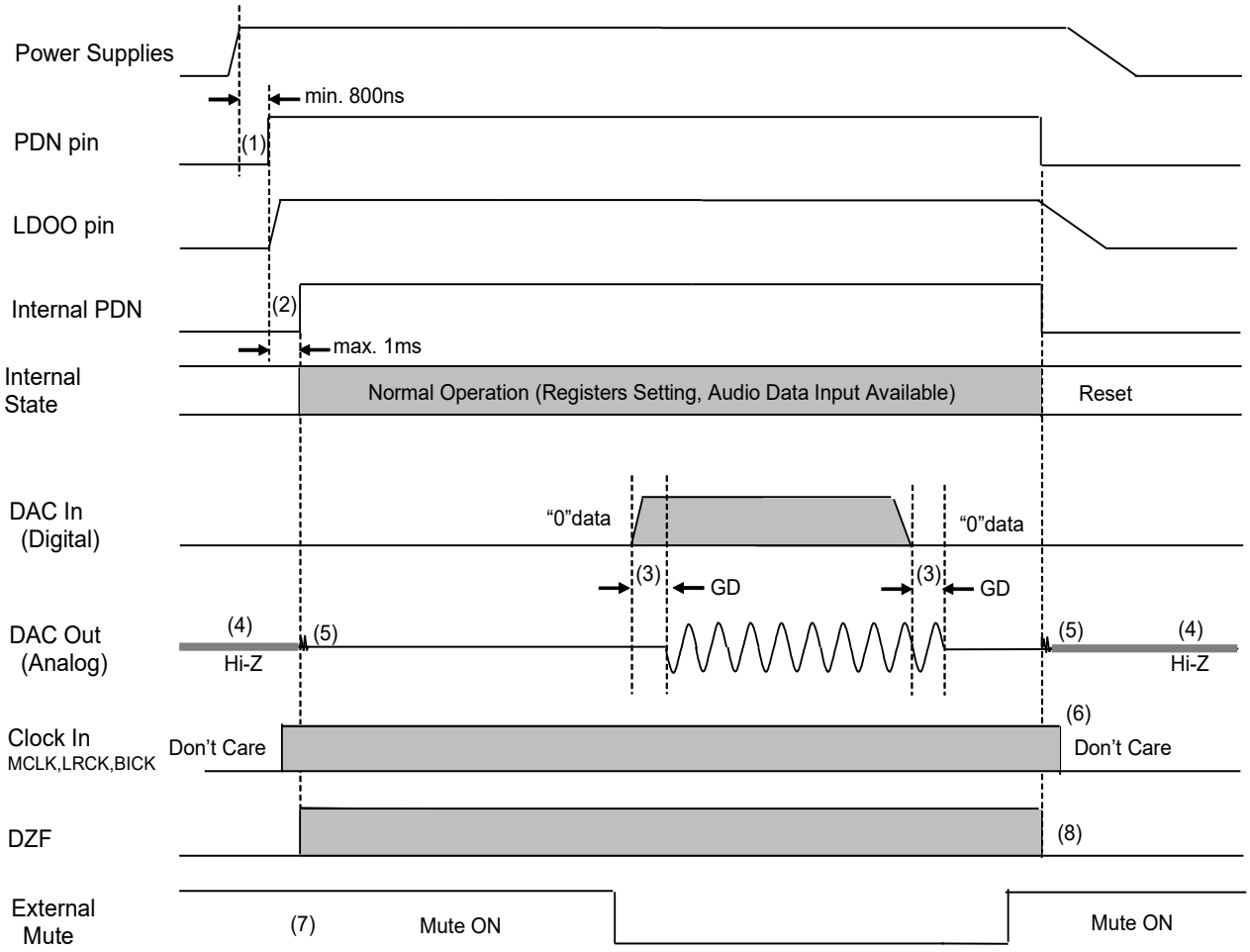
Three types of error can be detected (Table 19). When the error is detected, LDO is powered down and the digital core circuit stop. It will also be impossible to access to the control registers. When using the I^2C bus, the controller can know that an error has occurred because an ACK is not returned. Once the error is detected the AK4438 does not return to normal operation automatically even if the error condition is removed. So restart the AK4438 by the PDN pin.

No	Error Type	Error Condition
1	Internal Reference Voltage Error	Internal reference voltage is not powered up.
2	LDO Over Voltage Detection	LDO Voltage > 1.5V (typ.)
3	LDO Over Current Detection	LDO Current > 51mA (typ.)

Table 19. Error Types

12.11. Power Down Function

The AK4438 is placed in power-down mode by bringing the PDN pin “L”. In the power-down mode, all blocks are stopped in their initial state. The DAC outputs (AOUTL/R1–4 pins) become floating (Hi-Z) state. When powering up, set the PDN pin to “L” to initialize the AK4438. When the PDN pin is set to “H”, the power-down state is released, the reference voltages such as LDO and VCOM start up, and the control registers become accessible within 1 ms. Even after the PDN is set to “H”, the DAC1–4 remain stopped until MCLK and LRCK are input.
Power-up and power-down timings are shown in below.



Notes:
(1) After AVDD and TVDD are powered-up, the PDN pin should be “L” for 800ns.
(2) After PDN pin = “H”, the internal LDO and VCOM power-up. The internal registers are initialized. Register writing is available in 1msec after PDN pin = “H”.
(3) The DAC output corresponding to audio data input has group delay (GD).
(4) DAC outputs are floating (Hi-Z) in power down mode.
(5) Click noise occurs at an edge of internal PDN signal. This noise is output even if “0” data is input.
(6) MCLK, BICK and LRCK clocks can be stopped in power-down mode (PDN pin= “L”).
(7) Mute the DAC output externally if click noise (5) adversely affect system performance.
(8) The timing example is shown in this figure.
(9) The DZF pin outputs “L” in internal power-down mode.

Figure 30. Power Down/Up Sequence Example

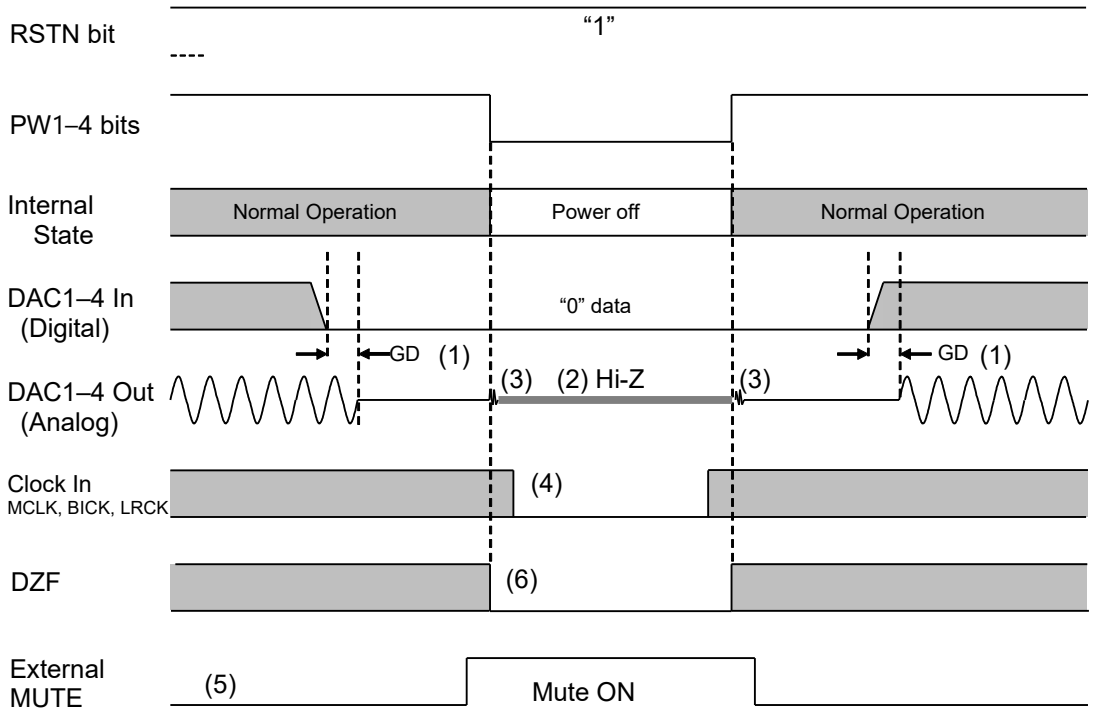
12.12. Power Off and Reset Functions

		Analog Output			
RSTN	PW4-1	DAC4	DAC3	DAC2	DAC1
0	0000	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	0001	Hi-Z	Hi-Z	Hi-Z	VCOM
0	0010	Hi-Z	Hi-Z	VCOM	Hi-Z
0	0011	Hi-Z	Hi-Z	VCOM	VCOM
0	0100	Hi-Z	VCOM	Hi-Z	Hi-Z
0	0101	Hi-Z	VCOM	Hi-Z	VCOM
0	0110	Hi-Z	VCOM	VCOM	Hi-Z
0	0111	Hi-Z	VCOM	VCOM	VCOM
0	1000	VCOM	Hi-Z	Hi-Z	Hi-Z
0	1001	VCOM	Hi-Z	Hi-Z	VCOM
0	1010	VCOM	Hi-Z	VCOM	Hi-Z
0	1011	VCOM	Hi-Z	VCOM	VCOM
0	1100	VCOM	VCOM	Hi-Z	Hi-Z
0	1101	VCOM	VCOM	Hi-Z	VCOM
0	1110	VCOM	VCOM	VCOM	Hi-Z
0	1111	VCOM	VCOM	VCOM	VCOM
1	0000	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	0001	Hi-Z	Hi-Z	Hi-Z	Normal
1	0010	Hi-Z	Hi-Z	Normal	Hi-Z
1	0011	Hi-Z	Hi-Z	Normal	Normal
1	0100	Hi-Z	Normal	Hi-Z	Hi-Z
1	0101	Hi-Z	Normal	Hi-Z	Normal
1	0110	Hi-Z	Normal	Normal	Hi-Z
1	0111	Hi-Z	Normal	Normal	Normal
1	1000	Normal	Hi-Z	Hi-Z	Hi-Z
1	1001	Normal	Hi-Z	Hi-Z	Normal
1	1010	Normal	Hi-Z	Normal	Hi-Z
1	1011	Normal	Hi-Z	Normal	Normal
1	1100	Normal	Normal	Hi-Z	Hi-Z
1	1101	Normal	Normal	Hi-Z	Normal
1	1110	Normal	Normal	Normal	Hi-Z
1	1111	Normal	Normal	Normal	Normal

Table 20. Power Off and Reset Function

12.12.1. Power OFF Function (PW1–4 bits)

When the PWx bit (x = 1–4) is set to “0”, the DACx is powered off. In power-off state, both digital block and analog block of DACx are stopped, and DACx outputs (AOUTL/Rx pins) are floating state (Hi-Z) (Table 20). Setting the PWx bit to “0” does not initialize the control registers. Figure 31 shows an example of system timing at power-off and power-on.

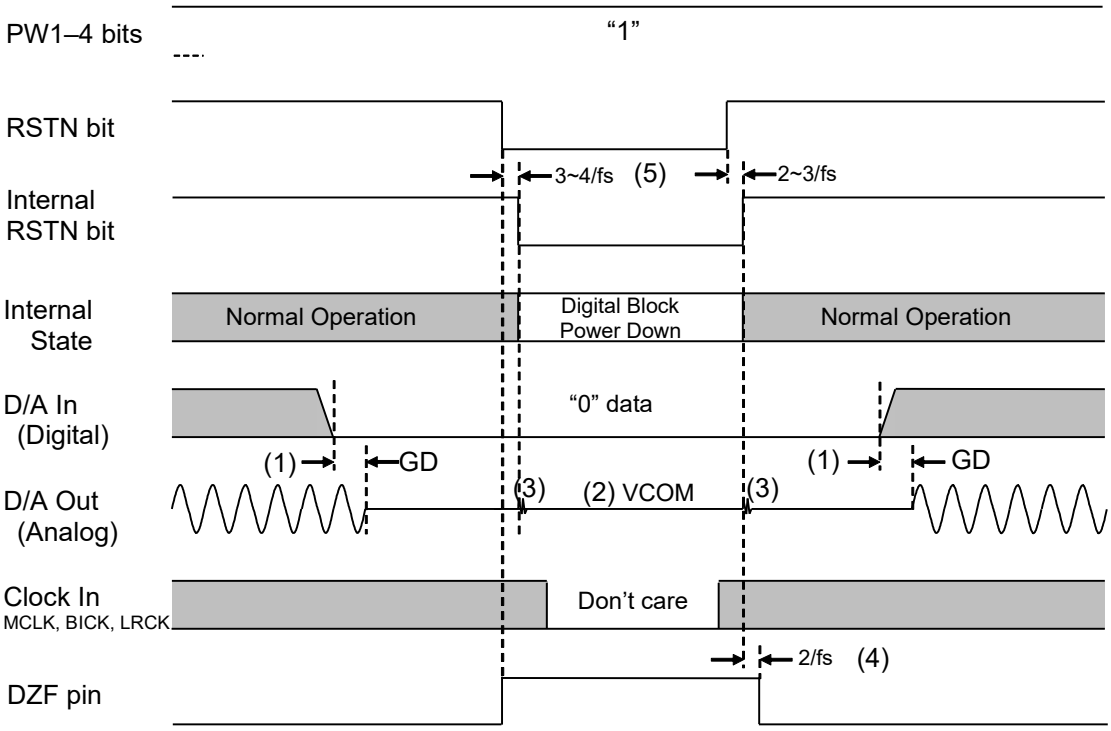


Notes:
(1) The DAC outputs corresponding to audio data input have group delay (GD).
(2) DACx output is floating (Hi-Z) in power-off state (PWx bit = “0”).
(3) Click noise occurs at the timing of the PWx bit change. This noise is output even if “0” data is input.
(4) If PW1–4 bits are all “0”, no blocks require the clocks (MCLK, BICK, LRCK), so there is no problem in stopping the clocks.
(5) Mute the DAC outputs externally if the click noise (3) adversely affects system performance.
(6) The DZF pin outputs “L” when DAC1 to DAC4 are all in power-off state (PW1–4 bits = “0000”).

Figure 31. Power-off/on Sequence Example

12.12.2. Reset Function (RSTN bit)

The DAC1–4 can be reset by setting RSTN bit to “0”. In this time, the DAC outputs (AOUTL/R1–4 pins) go to VCOM and the DZF pin outputs “H” if clocks (MCLK, BICK and LRCK) are input. The control register is not reset by setting RSTN bit to “0”. Figure 32 shows an example of reset sequence by RSTN bit.

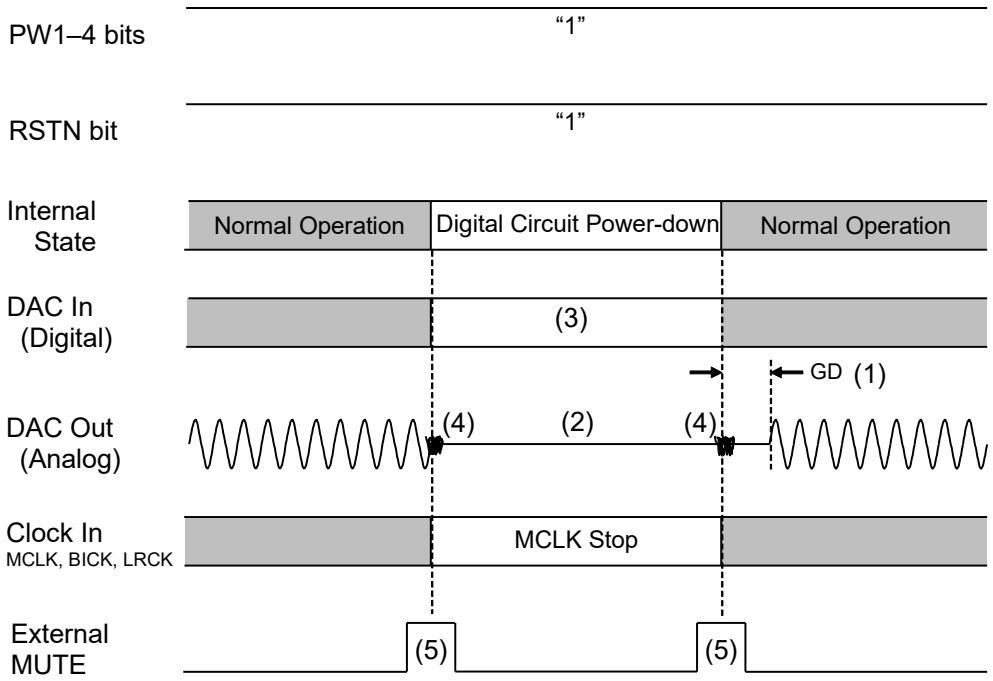


Notes:
(1) The DAC outputs corresponding to audio data input have group delay (GD).
(2) DAC outputs are VCOM voltage when RSTN bit = “0”.
(3) Click noise occurs at the edges (“↑ ↓”) of the internal RSTN. This noise is output even if “0” data is input.
(4) The DZF pin goes to “H” on the falling edge of RSTN bit and goes to “L” in 2/fs after a rising edge of the internal RSTN.
(5) There is a delay, 3–4/fs from setting RSTN bit to “0” to the internal RSTN goes to “0”, and 2–3/fs from setting RSTN bit to “1” to the internal RSTN goes to “1”.

Figure 32. Reset Sequence Example using RSTN bit

12.12.3. Reset Function (MCLK Stop)

The AK4438 is automatically placed in reset state when MCLK is stopped during normal operation, and the DAC outputs (AOUTL/R1–4 pins) go to VCOM voltage. When MCLK is input again, the AK4438 exits reset state and starts the operation. Zero detect function is disable when MCLK is stopped. Figure 33 shows an example of reset sequence by stopping MCLK.



Notes:
(1) The DAC outputs corresponding to audio data input have group delay (GD).
(2) When MCLK is stopped, DAC outputs go to VCOM voltage.
(3) Click noise after MCLK is input again can be reduced by inputting "0" data during this period.
(4) Click noise occurs within 3–4LRCK cycles from the MCLK stops and starts. This noise occurs even when "0" data is input.
(5) Mute the DAC outputs externally if click noise (4) influences system applications.

Figure 33. Reset Sequence Example using MCLK Stop

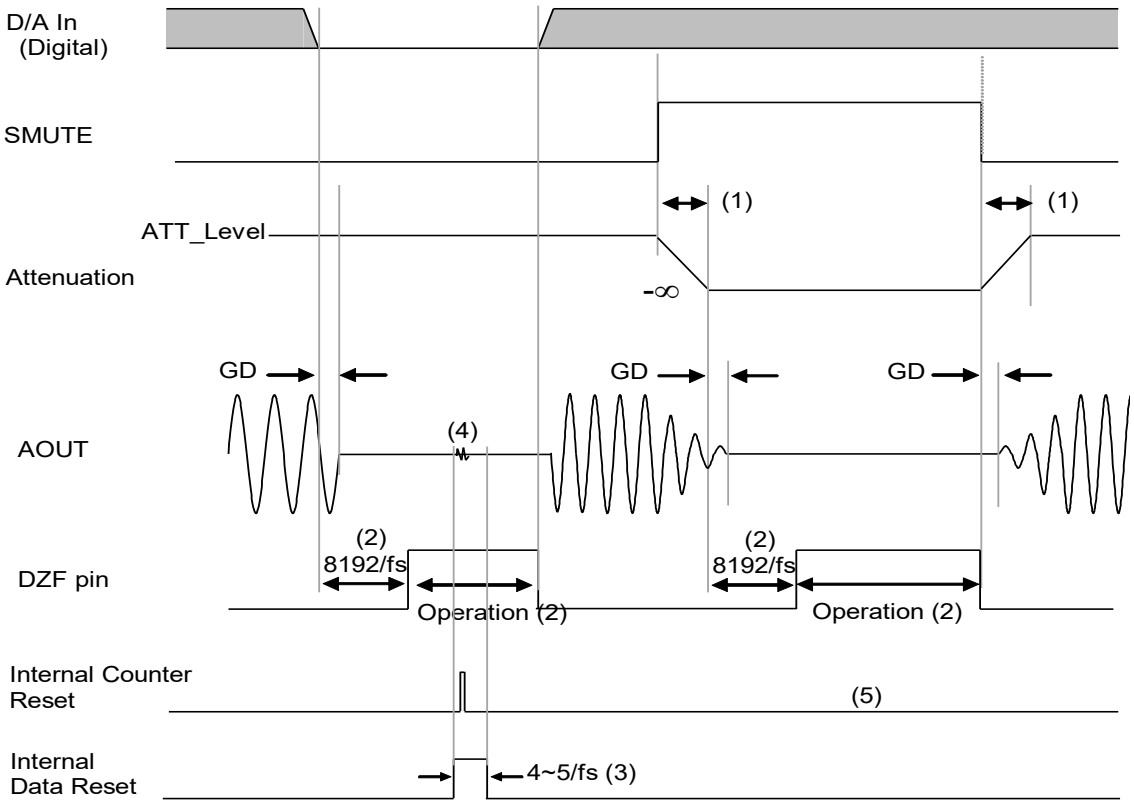
12.13. Clock Synchronization

The AK4438 has a function that resets the internal counter to keep a falling edge of the internal FSI clock is in 3/256fs from an edge of the external FSI clock. Clock synchronization function becomes valid when data at all channels are continuously “0” for 8192 times if SYNCE bit is set to “1” during operation in PCM mode or when RSTN bit is set to “0”. The operation clock is synchronized to a falling edge of LRCK in PCM mode and a rising edge of LRCK in I²C mode.

The analog output becomes VCOM voltage when RSTN bit = “0” or zero data is detected. Figure 34 shows a synchronization sequence when the input data is “0” for 8192 times continuously. Figure 35 shows a synchronization sequence by RSTN bit.

12.13.1. Clock Synchronization Sequence when Input Data is “0” for 8192 Cycles Continuously

The DZF pin goes to “H” and the synchronization function becomes enabled when input data is “0” for 8192 time continuously including when the data is attenuated. Figure 34 shows a synchronization sequence.

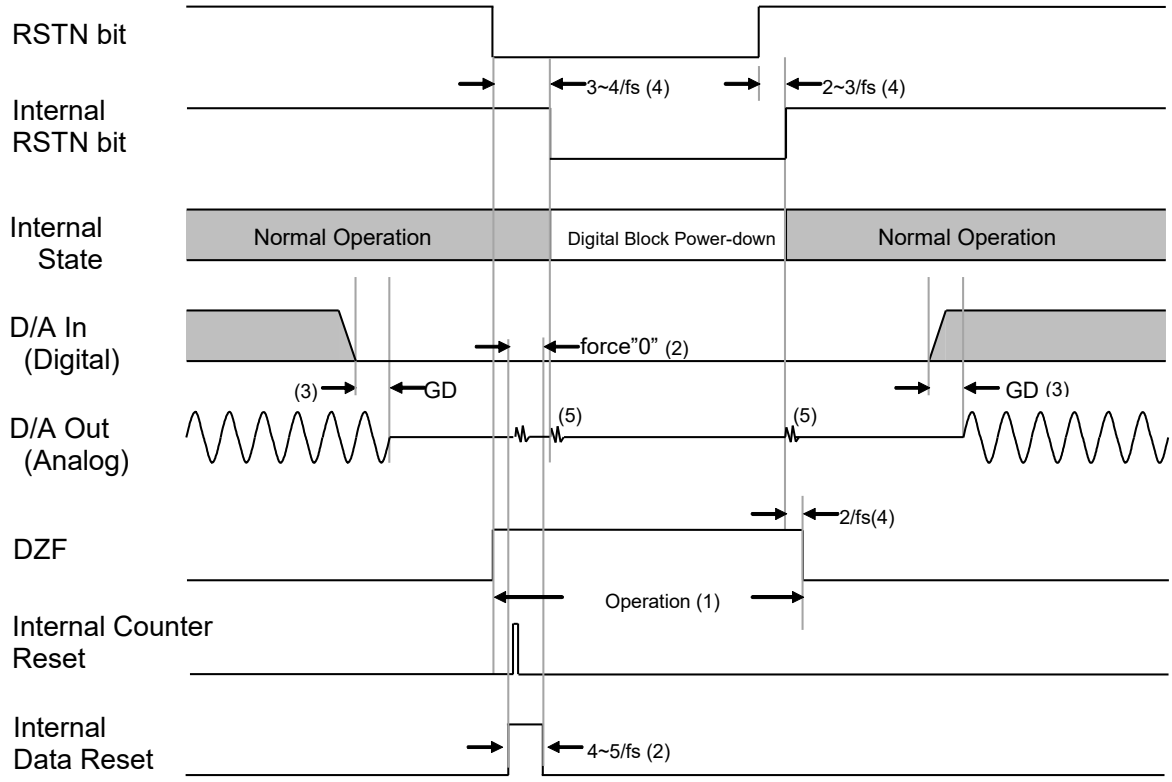


Notes:
(1) Refer to Table 14 internal transition time of ATT.
(2) The synchronization function becomes enabled when all channels input data are “0” for 8192 times continuously.
(3) Internal data is fixed to “0” for 4~5/fs forcibly when the internal counter is reset.
(4) Click noise occurs when the internal counter is reset. This noise is output even if “0” data is input. Mute the analog output externally if this click noise adversely affects system performance.
(5) The internal counter will not be reset when the internal and the external clocks are synchronized even if the synchronization function is enabled.

Figure 34. Clock Synchronization Sequence with Continuous Zero Data

12.13.2. Clock Synchronization Sequence with RSTN-bit

The DZF pin outputs “H” by setting RSTN bit to “0”. The DAC is reset after 3~4/fs from the DZF pin = “H”, and the analog output goes to VCOM voltage. The synchronization function is enabled when the DZF pin = “H”. Figure 35 shows synchronization sequence with RSTN bit.



Notes:

(1) The DZF pin outputs “H” by a falling edge of RSTN bit, and returns to “L” after 2/fs from the internal rising edge of RSTN bit. During this period the synchronization function is enabled.
(2) Internal data is fixed to “0” for 4~5/fs forcibly when the internal counter is reset.
(3) The analog output corresponding to digital input has group delay (GD). It is recommended that when writing “0” data to RSTN bit, “0” period should be longer than the GD period.
(4) It takes 3~4/fs to fall down and 2~3/fs to rise up for the internal RSTN signal from RSTN bit writing. There is a case that the internal counter is reset before internal RSTN bit is changed to “1” since the synchronization function becomes enabled immediately by setting RSTN bit = “0”.
(5) A click noise occurs by an internal RSTN signal edge or an internal counter reset. This noise is output even if “0” data is input. Mute the analog output externally if the click noise adversely affects the system performance.

Figure 35. Clock Synchronization Sequence with RSTN bit

12.14. Control Mode

The operation of AK4438 is controlled by pins or registers. There are three control modes: Parallel Control mode, 3-wire Serial Control mode, and I²C Bus Control mode. The control mode is selected by the I2C and PS pins. After changing the control mode, be sure to power down the AK4438 by setting the PDN pin to "L". If the power-down is not performed, the state before the change will not be initialized, which may lead to malfunction of the circuit.

I2C pin	PS pin	Control Mode
L	L	3w-Serial Control mode
L	H	3w-Serial Control mode
H	L	I²C Bus Control mode
H	H	Parallel Control mode

Table 21. Control Mode

12.14.1. Parallel Control mode

In Parallel Control mode, no register settings are required. The audio interface mode and soft mute function can be controlled via pins. Functions that cannot be configured by pins will operate under the default register settings. The system clock setting mode is forced to Auto Setting mode.（The default setting of register is Manual Setting mode.）

12.14.1.1. Audio Interface

The audio interface mode is set by the TDM1–0 and DIF pins (Table 22). Do not change TDM1–0, DIF pins during normal operation.

TDM1 pin	TDM0 pin	DIF pin	Mode in Table 9		Data Format
0	0	0	Normal	Mode6	32-bit MSB Justified
0	0	1		Mode7	32-bit I²S Compatible
0	1	0	TDM128	Mode12	32-bit MSB Justified
0	1	1		Mode13	32-bit I²S Compatible
1	0	0	TDM256	Mode18	32-bit MSB Justified
1	0	1		Mode19	32-bit I²S Compatible
1	1	0	TDM512	Mode24	32-bit MSB Justified
1	1	1		Mode25	32-bit I²S Compatible

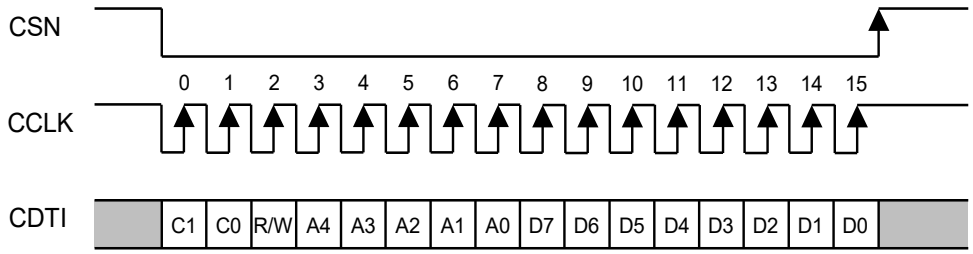
Table 22. Audio Interface Mode in Parallel Control mode

12.14.1.2. Soft Mute

The soft mute operation is controlled by SMUTE pin (Figure 29).

12.14.2. 3-wire Serial Control mode

Write to the control registers by the CSN, CCLK, and CDTI pins. The data on the CDTI pin consists of chip address (2 bits, C1-0), read/write (1 bit, fixed to “1”, write only), register address (MSB first, 5 bits) and register data (MSB first, 8 bits). Controller outputs each bit at the CCLK falling edge and the AK4438 takes it in at the CCLK rising edge. The register data is written to the register at CSN rising edge. The frequency of CCLK is 5MHz (max). The control registers are initialized by setting the PDN pin = “L”.



C1-C0: Chip Address (C1 = CAD1 pin, C0 = CAD0_SPI pin)
R/W: READ/WRITE (Fixed to “1”, Write only)
A4-A0: Register Address
D7-D0: Register Data

Figure 36. 3-wire Serial Interface Timing

* 3-wire Serial Control mode does not support read command.
* When PDN pin = “L”, writing to the control register is not possible.
* If the number of rising edges of CCLK is 15 or less or 17 or more while CSN is "L", register data cannot be written.

12.14.3. I²C Bus Control mode

The AK4438 supports the fast-mode I²C-bus (max: 400kHz).

12.14.3.1. WRITE Operation

Figure 37 shows the register write sequence in I²C-Bus Control mode. Access from the master to the AK4438 begins with a START condition. The START condition is to change the SDA line from “H” to “L” while the SCL line is “H”. (Figure 43). The master sends START condition followed by the first byte, which consists of the 7-bit slave address and data direction bit (R/W). The upper 5 bits of the AK4438 slave address are fixed to “00100”. The next 2 bits are the chip address to select the IC to access. They are set by the CAD1 and CAD0_I2C pins (Figure 38). When the R/W bit is “0”, data is written to the AK4438. When the R/W bit is “1”, data is read from the AK4438. If the slave address matches, the AK4438 returns an acknowledge (ACK). The master must generate a clock pulse for AK4438 to return an ACK and release the SDA line during that clock pulse (Figure 44).

The second byte is sub-address (control register address of the AK4438). The sub-address is 8-bit, MSB first, and the upper 3 bits are fixed to "0" (Figure 39). The third byte onwards is the data to be written to the control register. The data is 8-bit, MSB first (Figure 40). The AK4438 returns an ACK every time receiving one byte. The data transfer is terminated by a STOP condition generated by the master. The STOP condition is to change the SDA line from “L” to “H” while the SCL line is “H” (Figure 43).

The AK4438 has an address counter. The master can write data to multiple registers at once. After sending one byte of data, if master sends more data without sending a stop condition, the data will be written to the register at the automatically incremented address. If the master sends next data after writing data to address “14H”, the data will be written to address “00H”.

The SDA line must remain in it state during the “H” period of the SCL line. The SDA line can change state between “H” and “L” only when the SCL line is “L” (Figure 45). Only for START and STOP conditions, the SDA line changes state while the SCL line is “H”.

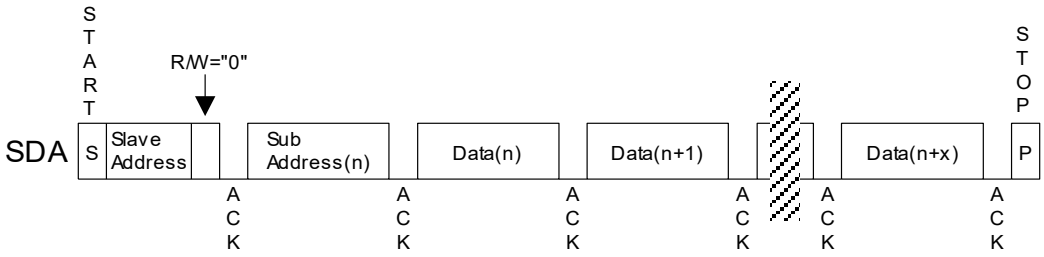


Figure 37. Write Sequence in I²C Bus Control mode

0	0	1	0	0	CAD1	CAD0	R/W

(CAD1 and CAD0 are determined by CAD1 and CAD0_I2C pin)

Figure 38. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 39. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 40. The Third Byte and subsequent bytes

12.14.3.2. READ Operation

When the R/W bit is “1”, the AK4438 outputs register data. The AK4438 has an address counter. If the master sends an ACK instead of a STOP condition after receiving one byte of register data, the AK4438 will output the register data at the automatically incremented address. After reading the data at address “14H”, if the master returns an ACK, the AK4438 outputs the data at address “00H”.

There are two read methods: Current Address Read and Random Address Read.

Current Address Read

When the master reads from the AK4438 without specifying a register address (sub-address), the AK4438 outputs register data according to the current value of the address counter. The counter holds the next address after the last accessed address. For example, if the last accessed address (either READ or WRITE) is "n-1", the AK4438 outputs register data of address "n" when the Current Address Read is performed. The AK4438 increments the counter after outputting the register data. If the master sends a STOP condition without returning an ACK after receiving the register data, the READ operation ends.

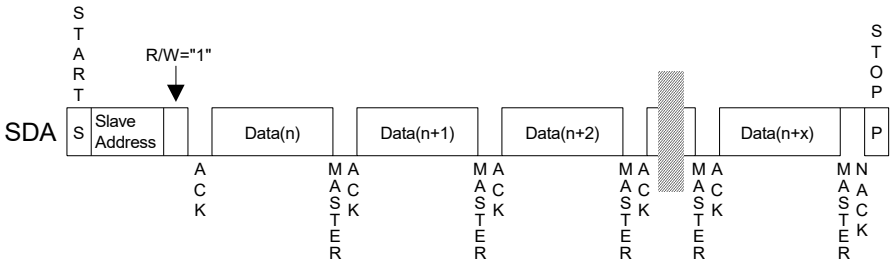


Figure 41. Current Address Read

Random Address Read

The Random Address Read is a method to read register data from any address. Write the sub-address “n” to the AK4438 before performing a READ operation. The address counter will be “n”. Then, when a READ operation is performed in the same way as the Current Address Read, the AK4438 outputs the register data sequentially from address “n”. If the master sends a STOP condition without returning an ACK after receiving the register data, the READ operation ends.

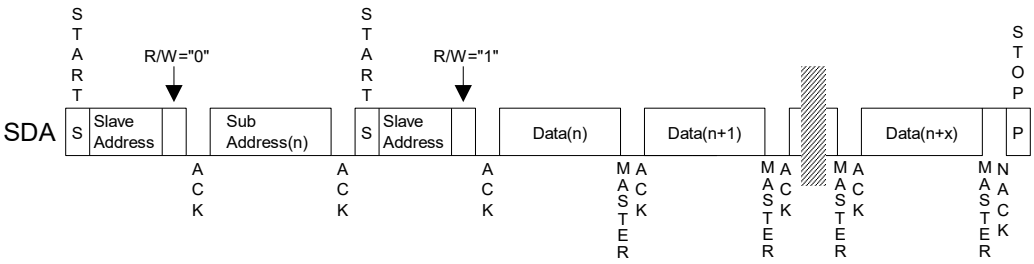


Figure 42. Random Address Read

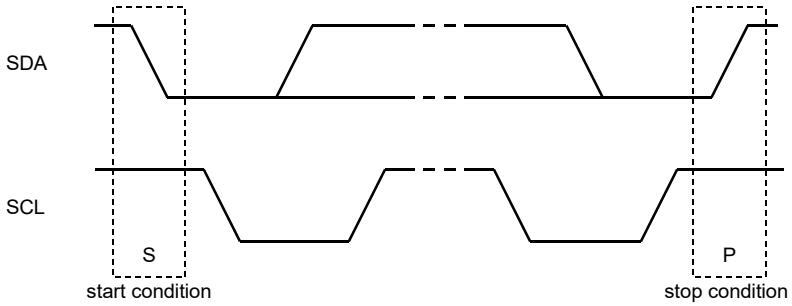


Figure 43. START and STOP Conditions

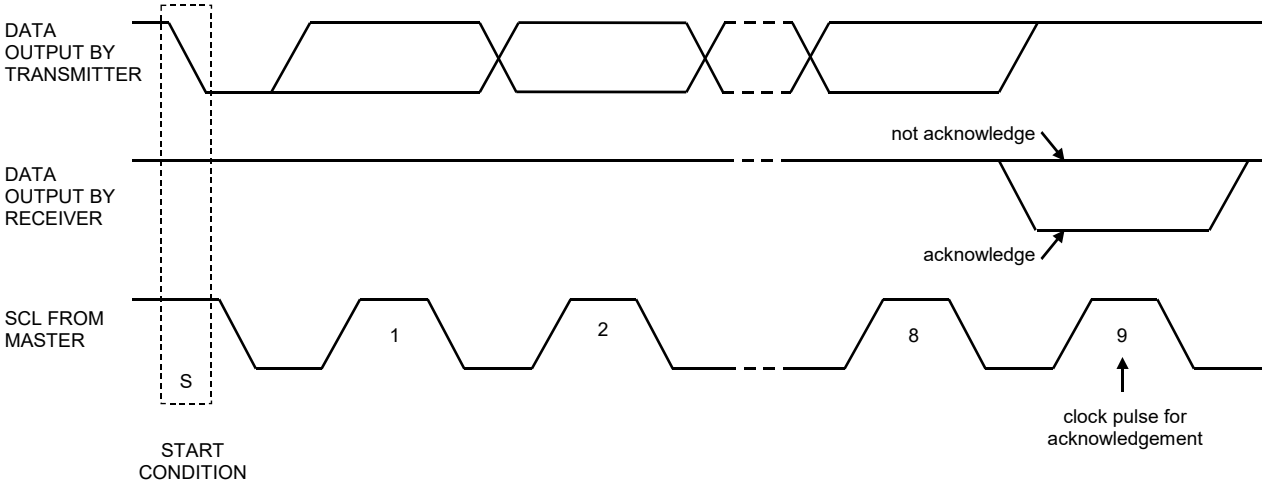


Figure 44. Acknowledge

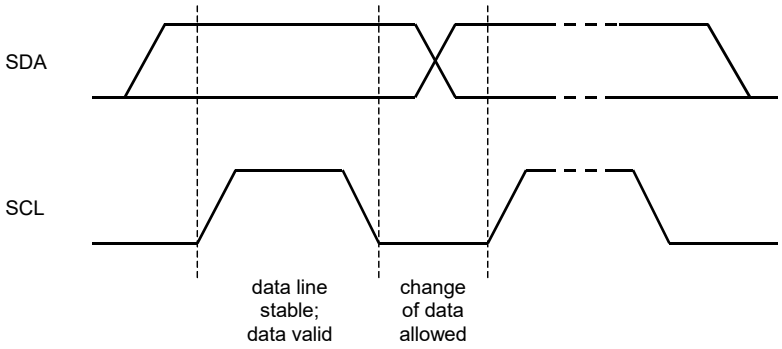


Figure 45. Bit Transfer on the I^2C-Bus

12.15. Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	0	0	SD	DFS1	DFS0	DEM11	DEM10	SMUTE
02H	Control 3	0	0	0	0	MONO1	DZFB	SELLR1	SLOW
03H	L1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	R1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	Control 4	INVL1	INVR1	INVL2	INVR2	SELLR2	0	DFS2	SSLOW
06H	-	0	0	0	0	0	0	0	0
07H	Control 6	L3	R3	L4	R4	0	0	0	SYNCE
08H	Control 7	L1	R1	L2	R2	0	0	0	0
09H	-	0	0	0	0	0	0	0	0
0AH	Control 8	TDM1	TDM0	SDS1	SDS2	PW2	PW1	DEM21	DEM20
0BH	Control 9	ATS1	ATS0	0	SDS0	PW4	PW3	0	0
0CH	Control 10	INVR4	INVL4	INVR3	INVL3	0	0	0	0
0DH	Control 11	MONO4	MONO3	MONO2	0	SELLR4	SELLR3	0	0
0EH	Control 12	DEM41	DEM40	DEM31	DEM30	0	0	0	0
0FH	L2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
10H	R2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
11H	L3ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
12H	R3ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
13H	L4ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
14H	R4ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

Notes:
(1) Data must not be written into addresses from 15H to 1FH.
(2) Write "0" to bits marked “0” and write "1" to bits marked “1”.
(3) When the PDN pin goes to “L”, the registers are initialized to their default values.
(4) When RSTN bit goes to “0”, the internal timing is reset, but registers are not initialized.

12.16. Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF2	DIF1	DIF0	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	1

RSTN: Internal Timing Reset
0: Reset
1: Normal Operation (default)

When this bit is set to “0”, the internal timing circuit is reset and the DZF pin goes to “H”. The registers are not initialized.

DIF2–0: Audio Interface Mode Select (Table 9)
default: “110” (mode 6 : Normal Input, 32-bit MSB Justified)

ACKS: Clock Setting Mode Select
0: Manual Setting mode (default)
1: Auto Setting mode
When ACKS bit = “1”, DFS2-0 bits setting not required.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	SD	DFS1	DFS0	DEM11	DEM10	SMUTE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	1	0

SMUTE: Soft Mute Control
0: Unmute (default)
1: Soft mute execution

DEM11–10: DAC1 De-Emphasis Filter Setting (Table 8)
default: “01” (De-Emphasis Filter OFF)

DFS2-0: Sampling Speed Mode Select (Table 1)
default: “000” (Normal Speed)
A click noise occurs when switching DFS2-0 bits setting.

SD: Short Delay Filter Enable (Table 11)
0: Sharp roll off filter or Slow roll off filter
1: Short delay Sharp roll off filter or Short delay Slow roll off filter (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	0	0	0	0	MONO1	DZFB	SELLR1	SLOW
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SLOW: Slow Roll-off Filter Enable (Table 11)
0: Sharp Roll-off Filter or Short Delay Sharp Roll-off Filter (default)
1: Slow Roll-off Filter or Short Delay Slow Roll-off Filter

SELLR1: Channel Swap Enable of DAC1 (Table 15)
0: No Swap (default)
1: Swap L, R channel

DZB: DZF pin Polarity Select (Table 12)
0: "H" at Zero Detection (default)
1: "L" at Zero Detection

MONO1: DAC1 Monaural Output Enable (Table 15)
0: Stereo Output (default)
1: MONO Output

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	L1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	R1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATT7–0: Attenuation Level Setting (Table 13)
default: "FFH" (0 dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Control 4	INVL1	INVR1	INVL2	INVR2	SELLR2	0	DFS2	SSLOW
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SSLOW: Super Slow Roll-off Filter Select (Table 11)
0: Other (default)
1: Super Slow Roll-off Filter

DFS2–0: Sampling Speed Mode Select (Table 1)
default: "000" (Normal Speed)
A click noise occurs when switching DFS2-0 bits setting.

SELLR2: Channel Swap Enable of DAC2 (Table 16)
0: No Swap (default)
1: Swap L, R channel

INVL1, INVR1: AOUTL1, AOUTR1 Output Phase Inverting (Table 15)
INVL2, INVR2: AOUTL2, AOUTR2 Output Phase Inverting (Table 16)
0: Normal (default)
1: Inverted

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Control 6	L3	R3	L4	R4	0	0	0	SYNCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

SYNCE: Clock Synchronization Enable
0: Disable
1: Enable (default)

L3, R3, L4, R4: AOUTL3/R3/L4/R4 Zero Detect Flag Enable
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Control 7	L1	R1	L2	R2	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

L1, R1, L2, R2: AOUTL1/R1/L2/R2 Zero Detect Flag Enable
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Control 8	TDM1	TDM0	SDS1	SDS2	PW2	PW1	DEM21	DEM20
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	1

DEM21–20: DAC2 De-Emphasis Filter Setting (Table 8)
default: “01” (De-Emphasis Filter OFF)

PW2: Power Management for DAC2
0: Power OFF
1: Power ON (default)

PW1: Power Management for DAC1
0: Power OFF
1: Power ON (default)

SDS2–0: Data Slot Assignment Select (Table 10)
default: “000” (DAC1: L1 and R1 Slot, DAC2: L2 and R2 Slot, DAC3: L3 and R3 Slot, DAC4: L4 and R4 Slot)

TDM1–0: TDM Mode Select (Table 9)
default: “00” (Normal Input)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Control 9	ATS1	ATS0	0	SDS0	PW4	PW3	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

PW4, PW3: Power Management for DAC4, DAC3
0: Power OFF
1: Power ON (default)

SDS2–0: Data Slot Select (Table 10)
default: “000” (DAC1: L1 and R1 Slot, DAC2: L2 and R2 Slot, DAC3: L3 and R3 Slot, DAC4: L4 and R4 Slot)

ATS1–0: Attenuation Level Transition Speed Select (Table 14)
default: “00” (4080/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Control 6	INVR4	INVL4	INVR3	INVL3	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

INVL3, INVR3: AOUTL3, AOUTR3 Output Phase Inverting (Table 17)
INVL4, INVR4: AOUTL4, AOUTR4 Output Phase Inverting (Table 18)
0: Normal (default)
1: Inverted

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Control 6	MONO4	MONO3	MONO2	0	SELLR4	SELLR3	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SELLR3: Channel Swap Enable of DAC3 (Table 17)
SELLR4: Channel Swap Enable of DAC4 (Table 18)
0: No Swap (default)
1: Swap L, R channel

MONO2: DAC2 Monaural Output Enable (Table 16)
MONO3: DAC3 Monaural Output Enable (Table 17)
MONO4: DAC4 Monaural Output Enable (Table 18)
0: Stereo Output (default)
1: MONO Output

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Control 6	DEM41	DEM40	DEM31	DEM30	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	0	0	0

DEM31–30: DAC3 De-Emphasis Filter Setting (Table 8)
DEM41–40: DAC4 De-Emphasis Filter Setting (Table 8)
default: “01” (De-Emphasis Filter OFF)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	L2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
10H	R2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
11H	L3ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
12H	R3ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
13H	L4ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
14H	R4ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATT7–0: Attenuation Level Setting (Table 13)
default: “FFH” (0 dB)

13. Recommended External Circuits

13.1. Typical Connection Diagram

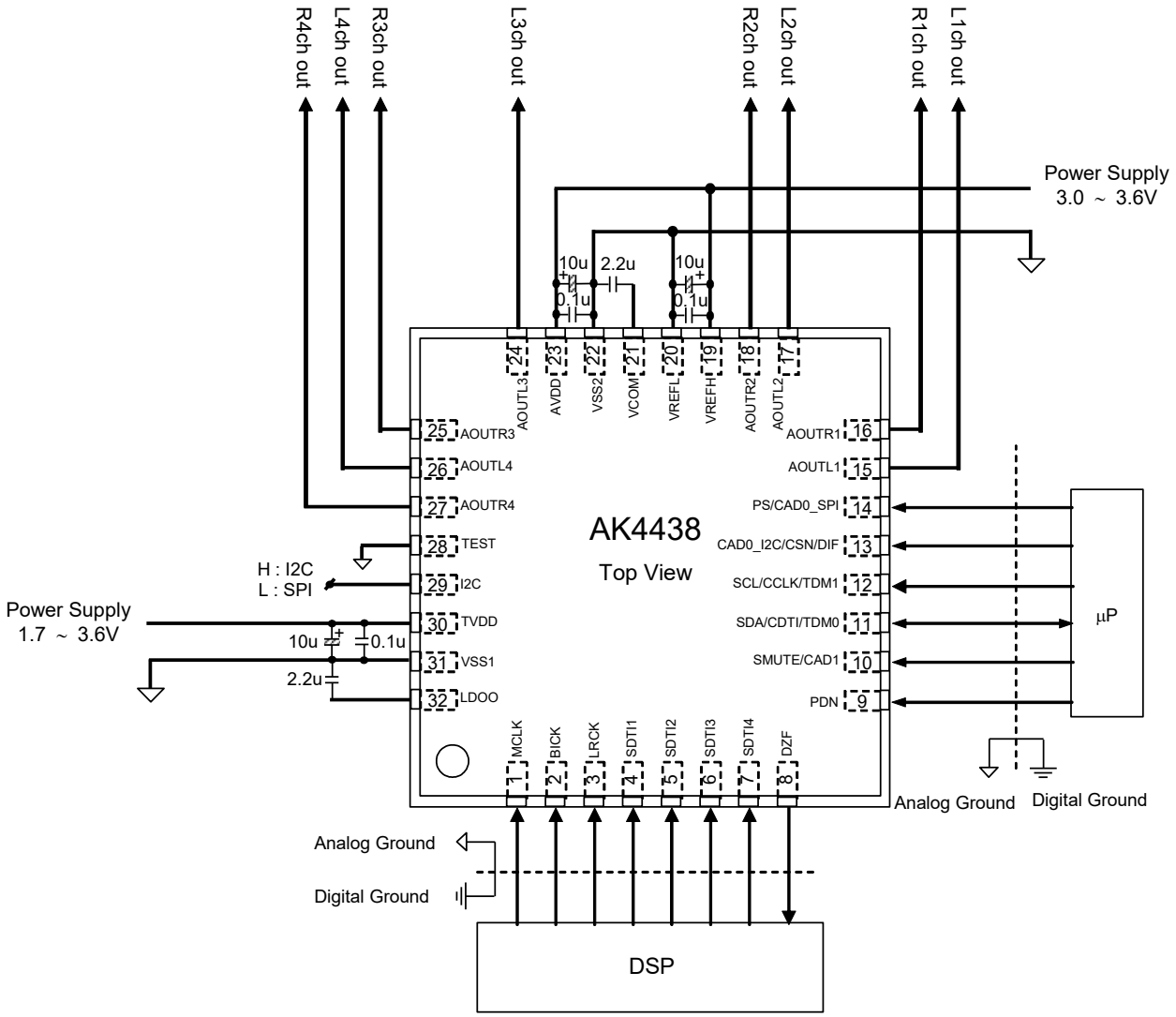


Figure 46. Typical Connection Diagram

Note: The AK4438 integrates smoothing filters.

13.1.1. Grounding and Power Supply Decoupling

The AK4438 requires careful attention to power supply and grounding arrangements. AVDD and TVDD are usually supplied from the analog supply of the system. If AVDD and TVDD are supplied separately, the power-up sequences between AVDD and TVDD is not critical. **VSS1 and VSS2 must be connected to the same analog ground plane.** System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4438 as possible.

13.1.2. Voltage Reference

The differential voltage between VREFH pin and VREFL pin sets the analog output range. The VREFH pin is normally connected to AVDD, and the VREFL pin is normally connected to VSS2. VREFHL and VREFL should be connected with a 0.1μF ceramic capacitor and 10μF electrolytic capacitor as near as possible to the pin to eliminate the effects of high frequency noise.
VCOM is a signal ground of this chip and output the voltage AVDDx1/2. A 2.2μF ±50% ceramic capacitor attached between the VCOM pin and VSS2 eliminates the effects of high frequency noise. This capacitor should be as close to the pin as possible. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VREFH pin and the VCOM pin in order to avoid unwanted coupling into the AK4438.
LDOO outputs 1.2V that is used for internal digital circuit. LDOO and VSS1 should be connected with a 2.2μF ±50% ceramic capacitor as near as possible to the pin to stabilize internal LDO. No load current may be drawn from the LDOO pin.

13.1.3. Analog Output

The output signal full scale is nominally 0.86 x VREFH Vpp centered around the VCOM voltage. The DAC input data is 2's complement. The output voltage is a positive full scale for 7FFFFFFFH(@32bit) and a negative full scale for 80000000H(@32bit). The ideal output is VCOM voltage for 00000000H(@32bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband.

13.1.4. External Analog Output Circuit

The output level of this circuit is 2.83Vpp (AK4438: typ. 2.83Vpp). Normally, DC component is cut by an external capacitor since the DAC outputs have DC offsets of a few millivolts to the VCOM voltage. The cutoff frequency of HPF is shown below.

$$fc = 1 / (2\pi \times R \times C) \text{ [Hz]}$$

Where the C is the external AC coupling capacitor, and the R is load resistance.
When C = 1μF and R = 10kΩ, then fs = 16Hz.

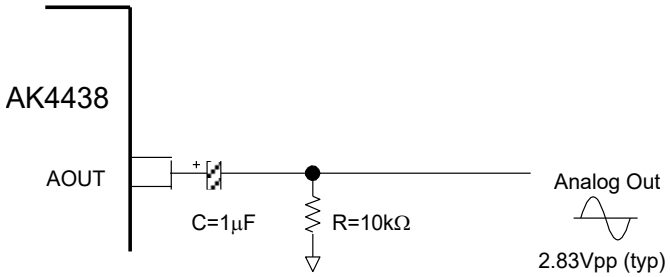
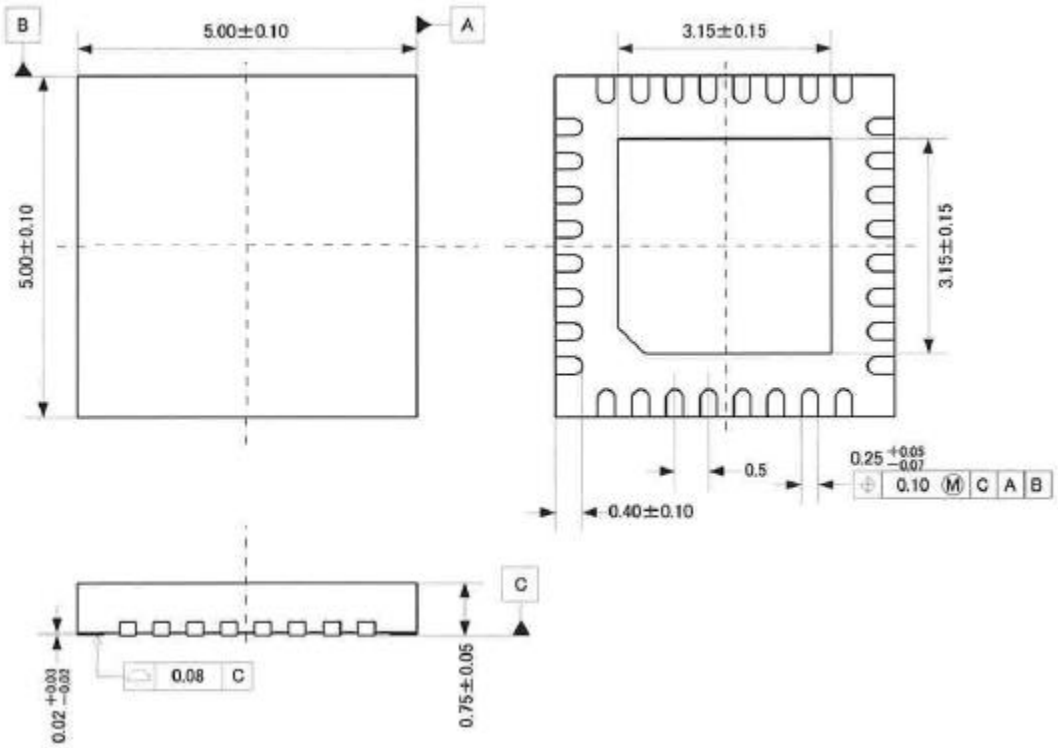


Figure 47. Output Circuit Example

14. Package

14.1. Outline Dimensions

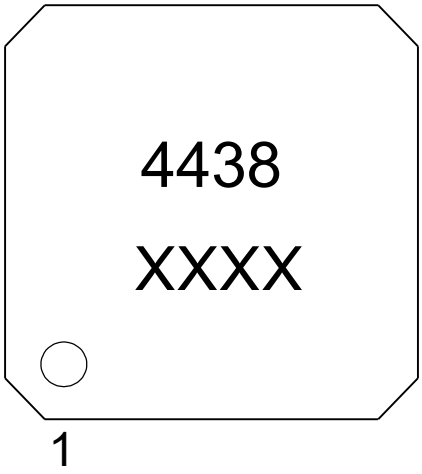
32-pin QFN (Unit: mm)



14.2. Material & Lead Finish

Package molding compound: Epoxy, Halogen (Br, Cl) free
Lead frame material: Cu
Terminal surface treatment: Solder (Pb free) plate

14.3. Marking



1) Pin #1 indication
2) Date Code: XXXX (4 digits)
3) Marking Code: 4438

15. Ordering Guide

AK4438VN	−40 °C – +105 °C	32-pin QFN (0.5mm pitch)
AKD4438	Evaluation Board for AK4438	

16. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
16/03/04	00	First Edition		
25/12/08	01	Error Correction	1	Features "Power Consumption" → "Current Consumption"
		Table Added	3	Block Diagram Add Block Function Table
		Error Correction	9, 11	Table of Sharp Roll-Off Filter, fs=96kHz Stopband typ. "0 kHz" → "-"
		Error Correction	15	Symbol in Table of Audio Interface Timing "tBLR" → "tLRB", "tLRB → tBLR"
		Error Correction	31	Figure 22. Mode 20/23/24 Timing "Mode 8" → "Mode20" "Mode 11, 12" → "Mode 23, 24"
		Error Correction	35	Table 23. Attenuation Level of Digital Volume Register "0A-11H" → "03H-04H, 0FH-14H"
		Error Correction	39	Error Detection Delete "when the LDOE pin = "H"."
		Error Correction	39	Table 18. Error Type "LDO Current < 51mA" → "LDO Current > 51mA"
		Error Correction	42	Figure 31. Power-off/on Sequence Example "PMDA3-1 bits" → "PW1-3 bits"
		Table Added	47	Control Mode Add Control Mode Setting Table
		Error Correction	55	Register Address 08H, D5, D4 "RD" → "R/W"
		Error Correction	59	Voltage Reference In the description about the LDO, "drawn from the VCOM pin" → "drawn from LDOO pin"
		Description Improvement	Overall	Unification of terminology and notation, correction of confusing descriptions.

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